MONOLITHIC INTEGRATION OF GERMANIUM-ON-INSULATOR PLATFORM ON SILICON SUBSTRATE AND ITS APPLICATIONS TO DEVICES

A DISSERTATION

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING

AND THE COMMITTEE ON GRADUATE STUDIES

OF STANFORD UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

Ju Hyung Nam

March 2016

Abstract

Due to its higher carrier mobilities and lower optical bandgap, germanium (Ge) has been considered as an attractive material for high performance CMOS and optical applications. High performance electrical and optical devices have already been demonstrated on a germanium-on-insulator (GOI) platform. To employ high performance GOI devices side by side with a silicon (Si) CMOS circuitry, monolithic integration of GOI platform on Si is needed.

In this work, a lateral overgrowth technique for the monolithic integration of GOI on Si is demonstrated. Silicon dioxide (SiO_2) is used as a growth mask. Ge is over-laterally grown from the growth windows defined in the SiO_2 to form the GOI platform. The technique gives a high quality GOI platform.

Based on the lateral overgrowth approach, lateral p-i-n photodiode with excellent diode characteristics and high optical response is demonstrated.

On the lateral overgrowth GOI, p-i-n and metal-semiconductor-metal (MSM) photodiodes are demonstrated. Ge MSM photodiodes typically show high dark current, due to the strong metal Fermi level pinning. To suppress the high dark current, photodiode with metal-insulator-semiconductor (MIS) contact is demonstrated using titanium oxide as a Fermi level de-pinning layer. The MIS contact allows transport of electrons freely but blocks holes to reduce dark current.

Acknowledgments

I would like to express my sincere respect and appreciation to my research advisor, professor Saraswat. Many years have passed since I first stepped into his office. I cannot thank him enough for the constant support in every aspect of my PhD study he has shown over the years. I was very fortunate to join his research group, where he has created an ideal research environment. Studying in his group was a happy, memorable, and rewarding experience.

In undergrad school, I studied with one of professor Kamins' textbooks on device physics. I was pleasantly surprised and honored to meet professor Kamins at Stanford. He helped me through all the difficulties in processes, integrations, and characterizations. Without his help and advice, many parts of my thesis works would have been difficult.

Many classes and lectures by professor Harris, forms the foundation of my understandings of semiconductor physics and optoelectronics. I frequented his office with questions on device physics; and later, to seek his advice in device fabrication and metrology. I deeply appreciate his advice and comments.

My understandings on transistors and CMOS industry comes largely from professor Wong. While taking his class early in my graduate career, I could grasp the workings of the semiconductor industry, and learned to perform literature searches to solve problems; in essence, I learned how to study as a graduate student. He has always been very encouraging whenever I sought his help and advice.

Professor Brongersma kindly advised and helped me with material/device characterizations and optical measurements. Throughout my study, I greatly relied upon his and his students' help on optical modeling and measurements. I would like to express my sincere appreciation on their help.

In every step of my work, I have always been helped by great colleagues. It has been a very rewarding experience to work with brightest of minds. In modeling, calculation, fabrication, characterization, and measurement, I always consulted and discussed with my fellow colleagues. We spent countless days and nights discussing, calculating, fabricating, and measuring together, and with them. I find those hours more exciting than tiring, and more thrilling than overwhelming. I only wish I could have been as helpful, as encouraging, and as supportive as my colleague were to me.

I was very fortunate to meet many great people during my study, and call them friends. With them, I make my years at Stanford full of fun and happy memories.

And to my family – I dare not find words to thank them for their unconditional love and support. Their love and encouragements were the biggest support to go through the years.

Table of Contents

List of tables

List of figures

Chapter 1:

Introduction: Germanium-on-insulator (GOI)

1.1Rise of germanium

The year of 2007 marked 60 years since the invention of the transistor. After the invention, transistors quickly overwhelmed existing electron tube based electronics and entirely changed everyday life. Personal computers, the Internet, and mobile devices are all based on transistor and miniaturization of integrated circuit technology. Over the 60 years, semiconductor industry saw tremendous success. In the year of 2009, about 10^{19} transistors were made and shipped. That is, on the average, 1 billion transistors for every person on Earth each year. This huge success of the semiconductor industry largely owes to the scalability of Si based CMOS devices. By scaling the dimension of CMOS devices, orders of magnitude faster operation speed, smaller size, and lower power consumption have been achieved. But as the dimension of the devices gets smaller and smaller, it is becoming increasingly difficult to achieve continued performance enhancements of the past five decades. To continue the device scaling with desired performance enhancements, boosting the channel mobility is needed. From the 90 nm technology node, the industry

has adopted SiGe source and drain stressors to strain the channel and boost the hole mobility in PMOS (Figure 1.1). Now, mobility enhancement from strain engineering is reaching its plateau, and the industry is looking for a new channel material.

Ge has been considered as one of the strongest candidates for high performance CMOS devices. Compared to Si, Ge has higher and more symmetric electron and hole mobilities, which lead to higher performance CMOS circuitry, with more symmetric and easier circuit design (Table 2.1). Compared to other options, e.g. III-V compound semiconductors, Ge is a group IV semiconductor as is Si, and when integrated on Si, there is no issue of cross-contamination and phase matching. Since SiGe is already in use for source and drain, Ge based devices can be easily integrated with already existing CMOS processes. Most notably, in 2015, by using SiGe as a channel material, the first 7 nm chip was demonstrated [1].

Scaling of the CMOS devices also requires scaling of the interconnect counterparts. With shrinking dimensions of metal interconnects and spacing between them, RC delay and power consumption rise and band width decreases. To overcome the issues, use of optical interconnects has been proposed. And optical interconnect system is composed of four parts: light sources, modulators, detectors and waveguides. As for the first three components, Ge is strongly considered as a building material. Because of its large indirect bandgap, Si cannot be used for light emission and due to large optical bandgap it not suitable for C-band 1550 nm optical interconnect systems. Some III-V compound semiconductors with direct bandgap could be used, but integration of the III-V based optical devices with Si CMOS circuitry is problematic. Ge, on the other hand, has low

optical bandgap of 0.66 eV, which can respond to 1550 nm optical signals especially with residual strain when integrated on Si (Figure 1.2).

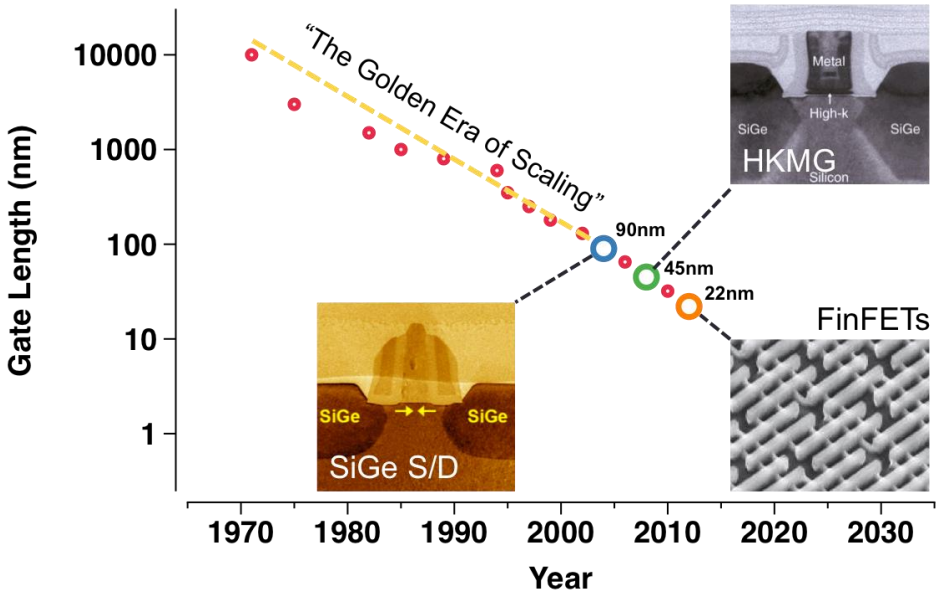

Figure 1.1. CMOS device scaling [2].

	Si	Ge	GaAs	InAs
Electron mobility	1600	3900	9200	40000
Hole mobility	430	1900	400	500
Bandgap (eV)	1.12	0.66	1.424	0.36

Table 1.1. Properties of bulk semiconductor materials.

Based on Ge, high performance optical detectors and modulators have already been demonstrated. Furthermore, its direct bandgap is only slightly larger than the indirect bandgap. With help of high tensile strain, light sources based on Ge is under very active research.

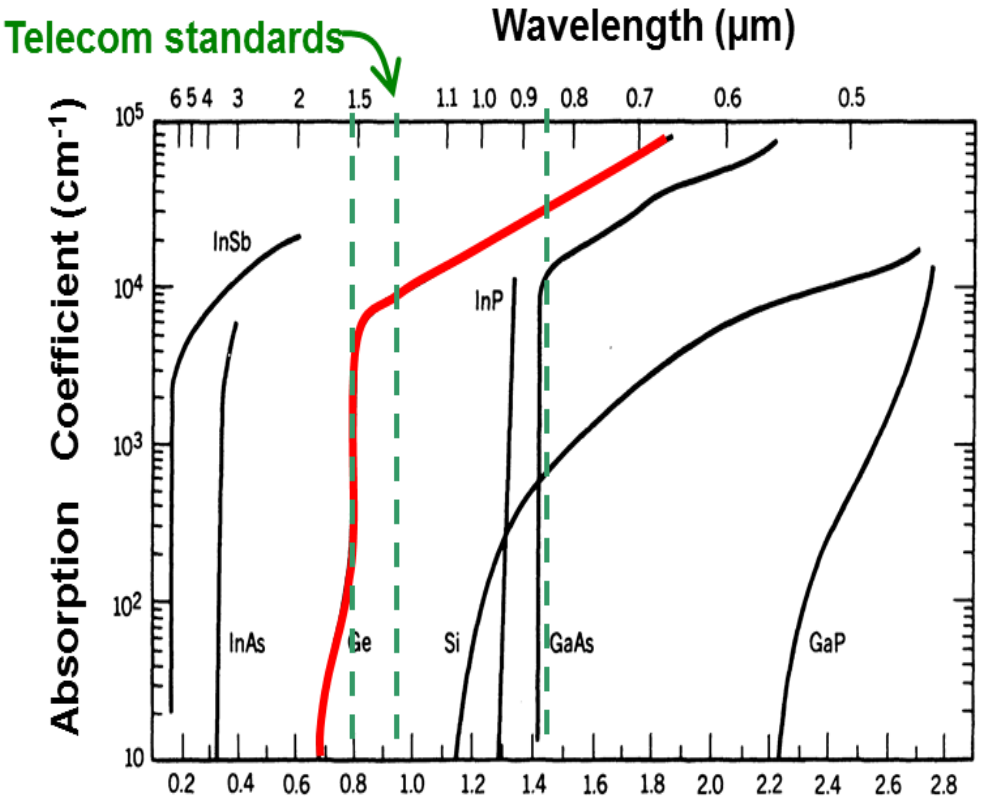

Figure 1.2. Bandgap of various semiconductor materials. Figure courtesy of Prof. K. C. Saraswat, Stanford University

1.2 Ge-on-insulator

Even though Ge has been considered as one of the strongest candidates for high performance CMOS applications and optical interconnects, it has a few drawbacks. Its low band gap leads to higher leakage current. When used for CMOS devices, its higher dielectric constant results in poor short channel effects (SCEs) [3-4]. To overcome these drawbacks while enjoying the benefits of Ge, use of Ge-on-insulator (GOI) has been proposed. For CMOS applications, GOI can provide better gate control and lower dark current. For optical devices, GOI provides electrical isolation between the Ge active layer and underlying Si substrate. For a Ge photodiode built directly on a Si substrate, when the diode is illuminated, photo carriers are generated in Ge. For shorter-wavelength optical interconnects, i.e., 850 nm system, the light is weakly absorbed in the Si substrate. Due to the long absorption length of Si at 850 nm (- 18 μm), photo carriers are generated deep inside the Si substrate. When the light is turned off, it takes long time for the deep-carriers to diffuse up to the contacts. This slows the response of the device, and limits the bandwidth of the system. By providing an electrical isolation, GOI based optical devices yield higher bandwidth [5-6]. Based on GOI platform, high performance optical devices have already been demonstrated [5-9].

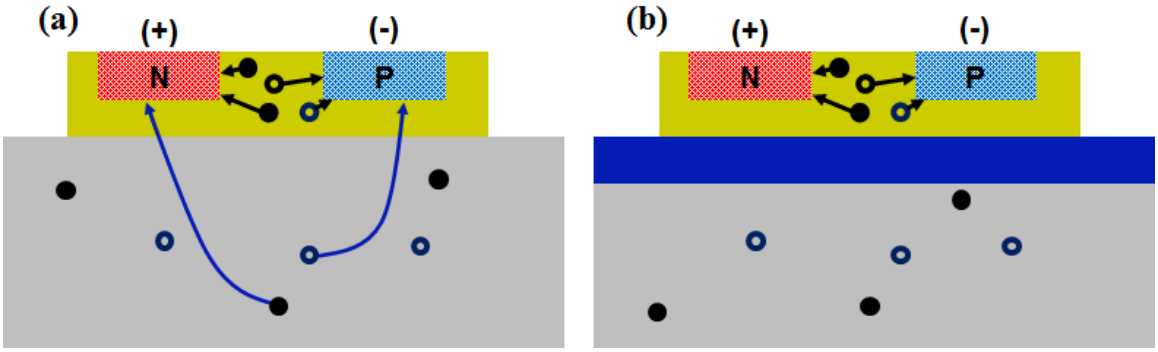

Figure 1.3. Carrier isolation by GOI.

1.3 Integration

GOI based electrical and optical devices show great promise to overcome difficulties nowadays industry is experiencing. Now, the question is how to integrate those GOI based devices with Si based CMOS circuitry. For the integration, several different approaches have been studied.

Most straightforward approach would be wafer bonding. In this approach, high crystal quality Ge is directly bonded onto an insulating layer. Leaving a thin Ge layer on insulator, Ge substrate is subsequently detached, and can be re-used for another run (Figure 1.4). Wafer bonding provides very high Ge crystal quality, but has several drawbacks. First of all, it cannot provide monolithic integration of Si based CMOS circuitry with GOI devices. And since the entire process has to start from an expensive GOI wafer, overall cost becomes higher compared to other approaches. Presence of Ge from the beginning also limits the Si processes. Furthermore, increasing wafer size makes

it increasingly difficult to achieve wafer bonding without defects. Instead of bonding Ge directly to an insulator, it can be directly grown on an ultra-thin Si-on-insulator (SOI) layer. This way, GOI devices can be monolithically integrated with SOI devices, but the price of the substrate is still higher compared to plain Si substrate. And when the GOI devices are built from this approach, Si based parasitic devices exist right beneath the Ge device, and degrades the device characteristics. Presence of a defective Si/Ge interface right beneath the Ge device also limits the device performance.

Rapid melt and growth (RMG) provides a monolithic integration of GOI with Si substrate [10]. Starting from a Si substrate, silicon nitride (Si_3N_4) is deposited, and patterned to define a seed region. Amorphous Ge is deposited and patterned to define GOI fingers. SiO_2 capping layer is deposited, and Ge is annealed till it melts. As the sample is cooled down, Ge re-crystallizes from the Si seed region and becomes a single crystal. Defects and dislocations are effectively collected near the necking region through defect necking. SiO_2 capping layer is removed, and the Ge layer is polished by chemical mechanical polishing (CMP). The crystalline Ge fingers sitting on Si_3N_4 can be used for GOI applications. RMG provides a means to monolithically integrate GOI with Si substrate (Figure 1.4), and through defect necking, the resulting crystal quality is high. Still, to ensure single crystalline Ge after the recrystallization, width of the GOI finger is limited. RMG shows poor thermal budget due to the high melting temperature of Ge (938.25 ℃). High annealing temperature also enhances Si/Ge inter-diffusion, which makes it difficult to have pure GOI without Si content [11-12]. RMG requires many

processing steps, including three steps of chemical vapor deposition (CVD), a couple of lithography steps, and a CMP.

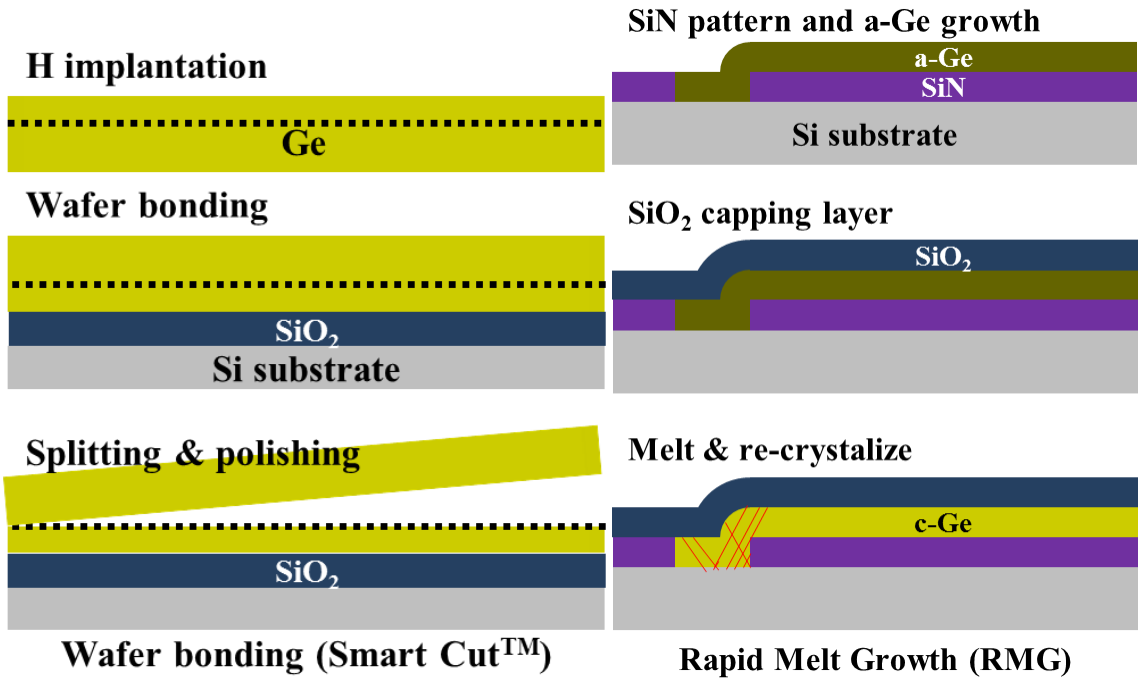

Figure 1.4. Integration of GOI: Wafer bonding and RMG.

For monolithic integration, lateral overgrowth has been proposed as an alternative. Lateral overgrowth is an extension of selective growth. Starting from a Si substrate, silicon dioxide (SiO_2) is either thermally grown or deposited by CVD. Growth windows are defined by optical lithography and dry etching. Ge is selectively grown through the growth window hetero-epitaxially. Once a growing Ge crystal fills up the growth window completely, Ge grows laterally over the SiO_2 growth mask. When neighboring Ge crystals coalesce on the SiO_2 growth mask and cover the entire growth window, Ge

surface is polished by CMP. Single crystalline Ge sitting on the SiO_2 growth mask can be used for the GOI applications (Figure 1.5). Lateral overgrowth provides an attractive means of monolithic integration of GOI on Si. Most importantly, the entire process is CMOS compatible. The process employs thermal oxidation of Si, optical lithography, dry etching, and epitaxial growth of Ge, all of which are already in use for standard CMOS process. With a relatively simple process, high quality GOI can be integrated on plain Si substrate by aspect ratio trapping (ART) and defect necking. But unlike selective growth of Ge on Si, since Ge on the SiO_2 growth mask is used as the device region, maintaining very high Ge growth selectivity over Si and SiO_2 is crucial. Also, neighboring Ge crystals coalesce at the middle of the GOI region, and due to the undercut usually formed at the growth front during the lateral growth of Ge on SiO_2 surface, a void region is usually formed at the coalescence point. To avoid this, fine control of Ge crystal growth is required.

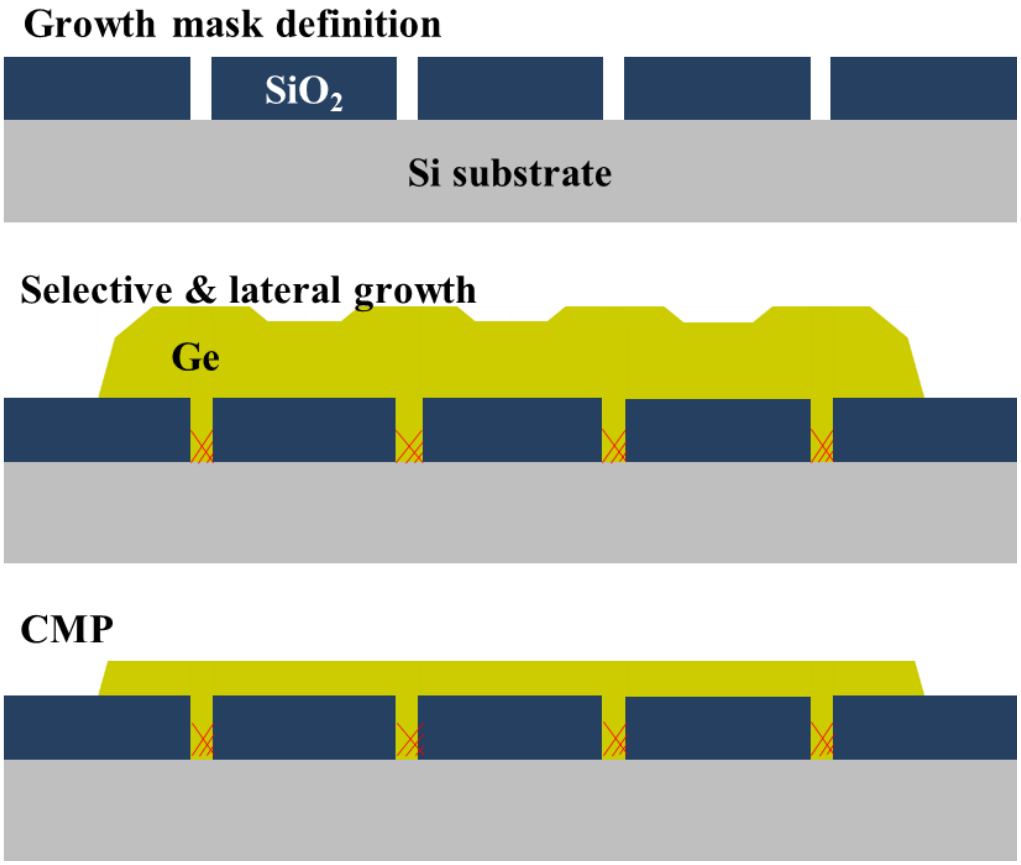

Figure 1.5. Lateral overgrowth of Ge for GOI.

1.4 Thesis organization

In Chapter 2, growth kinetics of Ge on Si during lateral overgrowth process is studied in detail. Based on the study, high crystal quality GOI platform monolithically integrated on a Si substrate is demonstrated and characterized.

In Chapter 3, a lateral overgrowth GOI based p-i-n photodiode with excellent diode characteristics and high optical response is demonstrated.

In Chapter 4, a metal-insulator-semiconductor Ge photodiode with low dark current, high optical response, and simple integration process is proposed and demonstrated.

Chapter 5 summarizes the main contributions of this thesis and proposes future works.

REFERENCE

[1] C. Vu, "IBM Research Alliance Produces Industry's First 7nm Node Test Chips," IBM, retrieved from https://www.ibm.com/ (July 9 2015)

[2] W. Jung, "Fluorine passivation of defects in germanium devices," PhD thesis, Stanford University (2014)

[3] C.-T. Chung, C.-W. Chen, J.-C. Lin, C.-C. Wu, C.-H. Chien, G.-L. Luo, "First experimental Ge CMOS FinFETs directly on SOI substrate," in IEEE International Electron Devices Meeting (IEDM), 2012, 16.4.1-16.4.4

[4] D. Hisamoto, W.-C. Lee, J. Kedierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, C. Hu, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," IEEE Transactions on Electron Device 47 (12), 2320-2325 (2000)

[5] S. J. Koester, G. Dehlinger, J. D. Schaub, J. O. Chu, Q. C. Ouyang, A. Grill, "Germanium-on-insulator photodiodes," in IEEE International Conference on Group IV Photonics, 2005, 171-173

[6] S. J. Koester, J. D. Schaub, G. Dehlinger, J. O. Chu, "Germanium-on-SOI infrared detectors for integrated photonic applications," IEEE Journal of Selective topics in quantum electronics 12 (6), 1489-1502 (2006)

[7] M. Oehme, M. Kaschel, J. Werner, O. Kirfel, M. Schmid, B. Bahouchi, E. Kasper, J. Schulze, "Germanium on silicon photodetectors with broad spectral range," Journal of Electrochemical Society 157 (2), H14-H148 (2010)

[8] D. Feng, S. Liao, P. Dong, N.-N. Feng, H. Liang, D. Zheng, C.-C. Kung, J. Fong, R. Shafiiha, J. Cunningham, A. V. Krishnamoorthy, M. Asghari, "High-speed Ge photodetector monolithically integrated with large cross-section silicon-on-insulator waveguide," Applied Physics Letters 95, 261105 (2009)

[9] L. Vivien, J. Osmond, J.-M. Fedeli, D. Marris-Morini, P. Crozat, J.-F. Damlencourt, E. Cassa, Y. Lecunff, S. Lacal, "42 GHz p.i.n germanium photodetector integrated in a silicon-on-insulator waveguide," Optics Express 17 (8), 6252-6257 (2009)

[10] Y. Liu, M. D. Deal, J. D. Plummer, "High-quality single-crystal Ge on insulator by liquid phase epitaxy on Si substrates," Applied Physics Letters 84, 2563 (2004)

[11] D. J. Tweet, J. J. Lee, J.-S. Maa, and S. T. Hsu, "Characterization and reduction of twist in Ge on insulator produced by localized liquid phase epitaxy," Applied Physics Letters 87, 141908 (2005)

[12] H. Y. S. Koh, "Rapid melt growth of silicon germanium for heterogeneous integration on silicon," PhD thesis, Stanford University (2011)

Chapter 2:

Lateral overgrowth of Ge on Si

As discussed in the previous chapter, lateral overgrowth is a very promising approach for monolithic integration of GOI based electrical and optical devices with Si based devices. The most basic technique required for the monolithic integration of GOI on Si using lateral overgrowth would be the hetero-epitaxial growth technique of Ge on Si. In this chapter, hetero-epitaxial growth technique to grow Ge on Si is briefly reviewed, followed by a detailed study on the lateral overgrowth process. Growth kinetics and growth models for the lateral overgrowth are studied, and a GOI platform by lateral overgrowth is demonstrated and characterized.

2.1 Hetero-epitaxial growth of Ge on Si

The very first step towards hetero-integration of Ge on Si would be growing high crystal quality Ge on Si. But there is 4.2 % lattice constant mismatch between the two materials, causing two challenges: layer-cluster growth and threading dislocations.

2.1.1 Growth mode and hydrogen annealing

Epitaxial growth of a film can be classified into three modes: layer-by-layer growth (Fank-van der Merwe growth), layer-cluster growth (Stranski-Krastanow growth), and cluster growth (Volmer-Weber), depending on the relative surface energies of the growing Ge film and the Si substrate, and the interface energy between the two. After a monolayer is grown, the growth mode can be determined by three terms: the surface energies of the substrate and the film, γ_s and γ_{fn}, respectively, and the interface energy, γ_{in}. Both γ_{fn} and γ_{in} vary with the Ge film thickness, due to the strain caused by the lattice constant mismatch between Ge and Si. If $\gamma_{fn} + \gamma_{in} < \gamma_s$ holds, layer-by-layer growth occurs [1]. Otherwise, layer-cluster growth or cluster growth occurs. For Ge growing on Si, in the beginning, Ge film wets the Si surface, but due to the lattice constant mismatch and the elastic energy stored in the film, γ_{in} increases with the growing thickness. When γ_{in} reaches the critical level, Ge islands form to release strain (Figure 2.1) [1-3]. Due to the 4.2 % lattice mismatch, critical thickness of Ge on Si is typically limited to ~4 monolayers, which is thinner than any practical requirements [4-5]. As a result, Ge grown on Si typically shows very rough surface with islands [6].

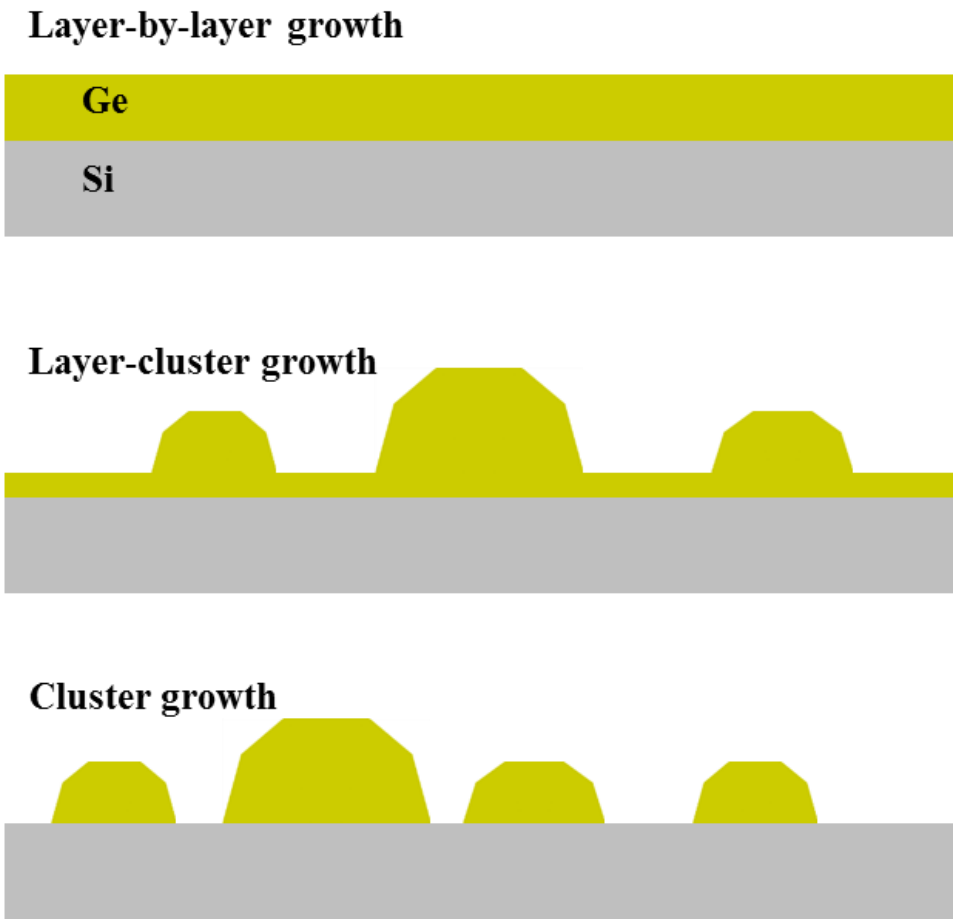

Figure 2.1. Three Ge growth modes on Si

To planarize the rough surface for device application, multiple hydrogen annealing for heteroexpitaxy (MHAH) has been demonstrated [6]. On a Si substrate, initial Ge layer is grown. On the rough surface, hydrogen annealing is done at high temperature. During the annealing, hydrogen-Ge cluster is formed, which lowers diffusion barrier, enhances diffusion, and increases surface mobility. As a result, hydrogen annealing drastically reduces the surface roughness. Successful reduction of surface RMS roughness on a 200

nm Ge layer from 24.964 nm to 2.947 nm by hydrogen annealing has been demonstrated [6]. On the planarized surface, second layer of Ge is grown, and annealed with hydrogen. The process is repeated until the desired thickness is reached [7]. MHAH allows the hetero-epitaxial growth of Ge on Si with planar surface.

2.1.2 Dislocations

In the beginning stage of the hetero-epitaxial growth process of Ge on Si, it is energetically favorable to grow in coherence with the Si lattice, without introducing energetically active defects. But, because of the lattice constant mismatch, the Ge layer gets strained, and as a result, elastic energy is stored in the Ge layer. As the layer grows thicker, the elastic energy increases. At certain thickness, called critical thickness, when the elastic energy overcomes the energetic expense of introducing dislocations, it becomes energetically favorable to relieve the strain by introducing misfit dislocations at the Si/Ge interface (Figure 2.2) [1-2]. At the end of each misfit dislocation, the misfit dislocation threads to a surface to form a half-loop, following (111) plane (Figure 2.3) [1].

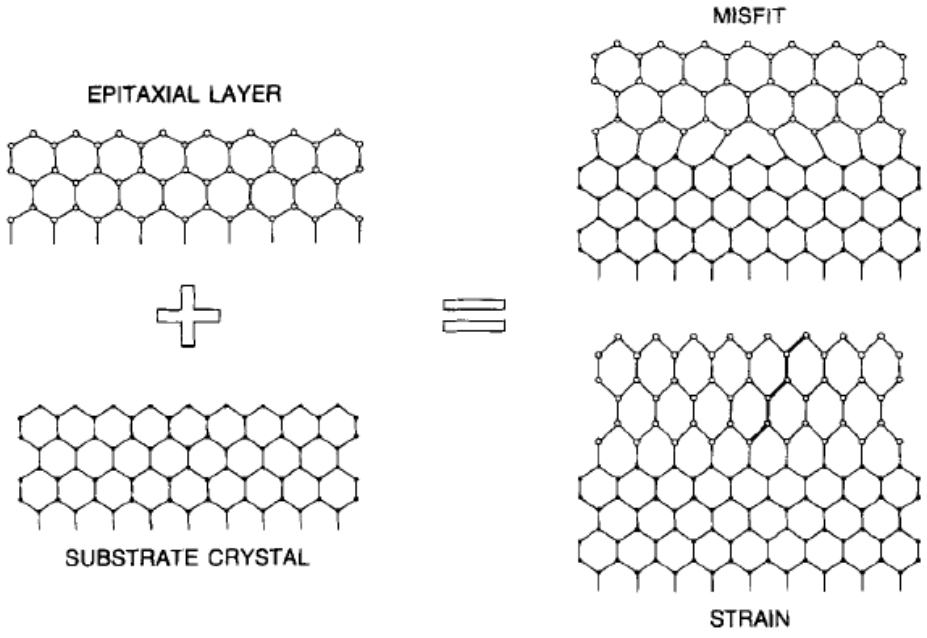

Figure 2.2. Hetero-epitaxial growth of Ge on Si. Reprinted with permission from [1]. Copyright 1999 Elsevier.

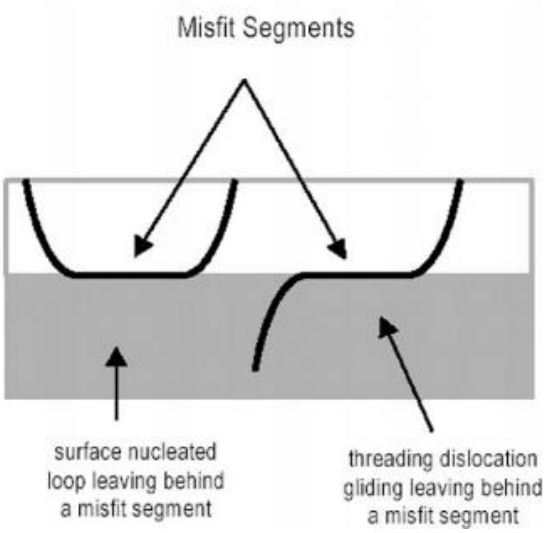

Figure 2.3. Misfit and threading dislocations. Reprinted with permission from [2]. Copyright 2003 Springer.

The atoms at the dislocations will not have normal 4-fold tetrahedral bonding, and cause carrier trapping and generation [1]. For high performance CMOS and optical devices, it is crucial to have high crystal quality Ge with low threading dislocation density [9].

What determines the threading dislocation density? Inside an epitaxial layer, a threading dislocation is a disturbance from the perfect crystalline structure, and generates a strain field. Other threading dislocations are affected by the strain filed, and experience an interaction force. In the epitaxial film, for a threading dislocation to move from one position to next valley, an energy barrier needs to be overcome. If the interaction is strong enough to overcome the energy barrier, the threading dislocation can move to the next valley. If the two threading dislocations have opposite Burgers vectors, then they move towards each other and annihilate. On the other hand, if the two threading dislocations have same Burgers vectors they move away from each other to the point when the interaction between the two becomes too weak to overcome the energy barrier. Following this model, equilibrium threading dislocation density (TDD) can be expressed as

$$\rho_{eq} = \left(\frac{2}{b}\left\{1 - exp\left[-\frac{2\pi(1-v)E_a}{\mu b^2 L(1 - v\cos^2\theta)}\right]\right\}\right)^2 \cong \left[\frac{4\pi(1-v)E_a}{\mu b^3 L(1 - v\cos^2\theta)}\right]^2,$$

where ρ_{eq} is the equilibrium TDD, b is Burgers vector length (fog Ge, 4 Å), ν is Poisson ratio (for Ge, 0.273), E_a is the barrier energy (for Ge, 1.5 eV), μ is the shear modulus of the epitaxial film (for Ge, 67.0 GPa), L is the threading dislocation length, which is equal to the film thickness, and θ is the angle between the Burgers vector and the dislocation

line direction (60 °) [10]. The expression shows TDD is a function of the layer thickness L, and as the layer grows thicker, TDD gets smaller. Resulting TDD as a function of film thickness is plotted in Figure 2.4.

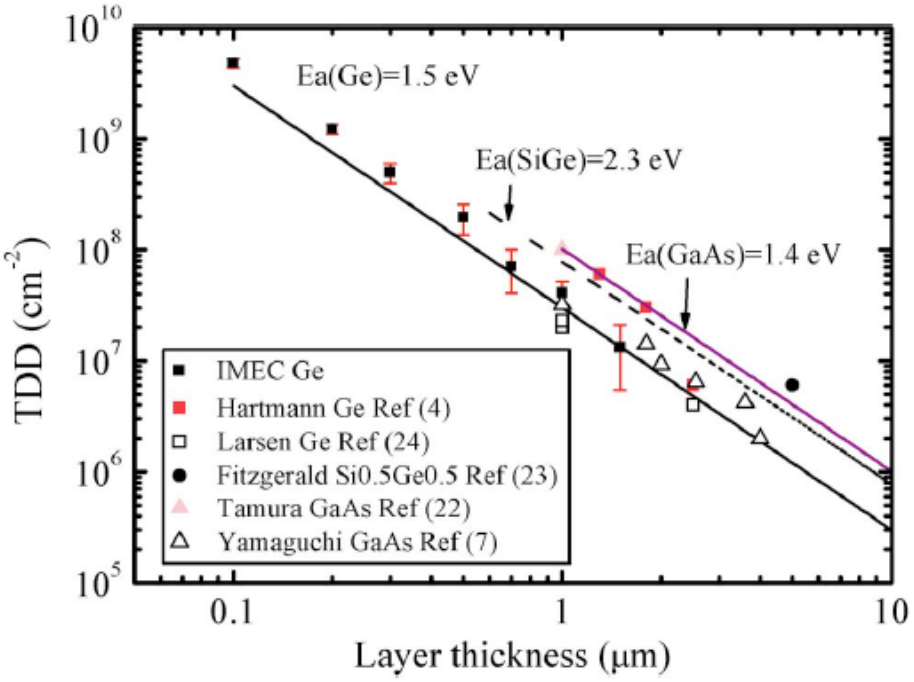

Figure 2.4. Equilibrium TDD as a function of film thickness. Reprinted with permission from [10]. Copyright 2009 AIP Publishing LLC.

To further lower the TDD and improve crystal quality of the epitaxial film, aspect ratio trapping (ART) has been proposed. This can be achieved by growing Ge through a high aspect ratio growth window, by using SiO_2 as a growth mask.

To locally produce Ge based devices on Si, a selective growth technique is needed. This is typically achieved by using SiO_2 as a growth mask. On a Si substrate, SiO_2 layer

is either thermally grown or deposited. Growth windows are defined by locally revealing the Si surface, by lithography and dry etching. SiO_2 serves as a growth mask, and Ge growth can be confined within the growth window. By using SiO_2 as a growth mask, high performance Ge devices have been locally integrated on a Si substrate [11-13].

On a Si (001) substrate, threading dislocations propagate on (111) planes following <011> direction, 45 ° off from the Si (001) surface [14]. During the selective growth, by defining aspect ratio of the growth window greater than 1, it is possible to terminate the threading dislocations propagating form the Si/Ge interface at the SiO_2 growth window sidewall, leaving the Ge surface free of threading dislocations [14] (Figure 2.5). By ART, high crystal quality Ge has been achieved [14], and high performance Ge devices have been demonstrated [15].

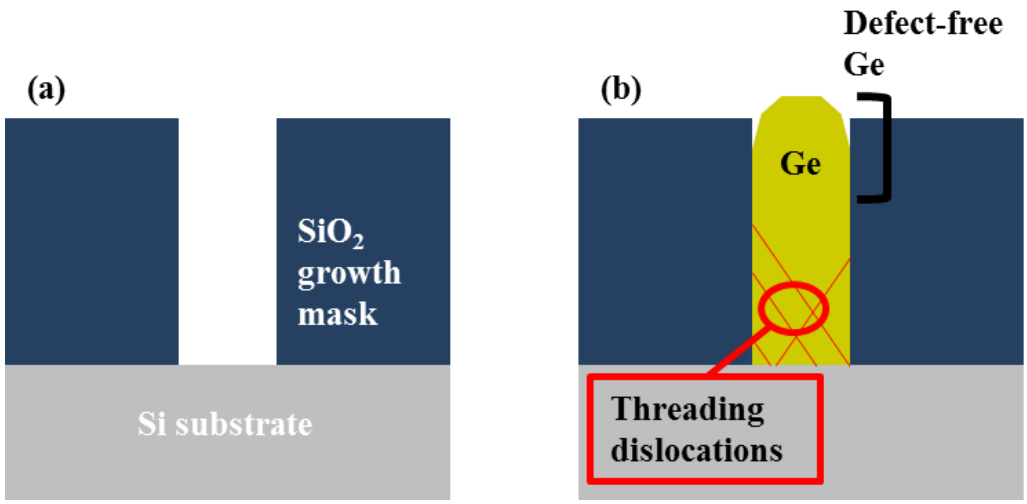

Figure 2.5. Aspect ratio trapping. (a) Growth window definition and (b) Ge growth with trapping of threading dislocations by the SiO_2 side wall.

2.2 Lateral overgrowth

By MHAH and ART, high crystal quality Ge can be grown hetero-epitaxially on Si. Going one step further, for the integration of GOI based devices on a Si substrate, lateral-overgrowth has been proposed [16-17].

2.2.1 Lateral overgrowth process

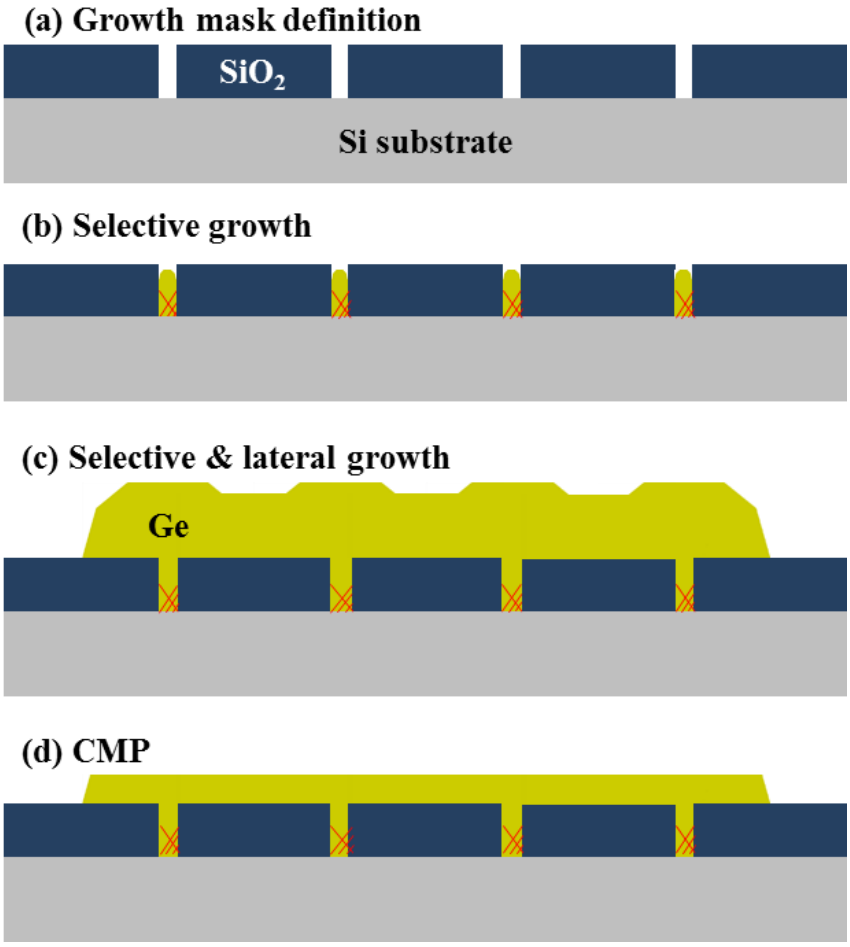

Figure 2.6. Lateral overgrowth of Ge for GOI.

Figure 2.6 shows the process flow of the lateral overgrowth. Starting from Si (001) substrate, thermal oxide is grown as the Ge growth mask. Growth windows are defined using optical lithography and dry etching. For better starting surface for the growth, dry etching is stopped 20 nm above the Si surface, and finished with wet etching using 20:1 HF. For ART, aspect ratio of the windows is kept bigger than 1. The mask edges are aligned along <110> direction (Figure 2.6. (a)).

From the growth window, Ge is grown hetero-epitaxially. The sample is prepared by an HF-last RCA cleaning, and immediately loaded into an Applied Materials Centura epitaxial reactor. To remove any remaining native oxide inside the growth window, the sample is baked at 1000 ℃ in hydrogen (H_2). For a better quality seed layer, a thin Si layer is grown selectively on the exposed Si growth windows using dichlorosilane (DCS). Then Ge is grown selectively from the growth window, using germane (GeH_4) gas.

For better step coverage [1], 100 nm Ge seed layer is grown at low temperature (400 ℃). The growth is done by 30 sccm of GeH_4 at 30 Torr, for 300 sec. After the seed layer growth, high temperature H_2 annealing is done at 825 ℃. The cycle is repeated twice (Figure 2.5. (b)). On the selectively grown Ge seed layer, Ge is selectively and over-laterally grown further under different conditions (Figure 2.6. (b)-(c)). After the coalescence of neighboring Ge crystals, <001> directional growth becomes dominating, and quickly fills up the valleys. CMP is done to planarize the GOI surface, and control the GOI layer thickness (Figure 2.6. (d)) [18-20].

Typically, lateral overgrows suffers from two limitations: 1) poly-crystalline Ge nucleation on SiO_2 growth mask, and 2) void formation at the center of the GOI region [7, 18-20].

Due to the limited growth selectivity of SiO_2, during the selective and lateral growth of Ge, poly-crystalline Ge nuclei are grown on SiO_2 growth mask. This poly-crystalline Ge degrades crystal quality of the GOI. Not like the selective growth, lateral-overgrowth uses Ge on SiO_2 as the device area, for device applications, it is crucial to suppress poly-crystalline nucleation (Figure 2.7. (a)).

When a Ge crystal grows over-laterally on SiO_2 surface, due to the high interface energy between Ge and SiO_2, negative-sloped undercuts are formed at its growth fronts. Due to the undercuts, when neighboring Ge crystals coalesce on the SiO_2 surface, a void is formed at the center of the GOI region. This void makes device applications complicated.

For lateral overgrowth GOI to be used for high performance device applications, it is crucial to suppress poly-crystalline Ge nucleation, and eliminate the void region (Figure 2.7. (b)).

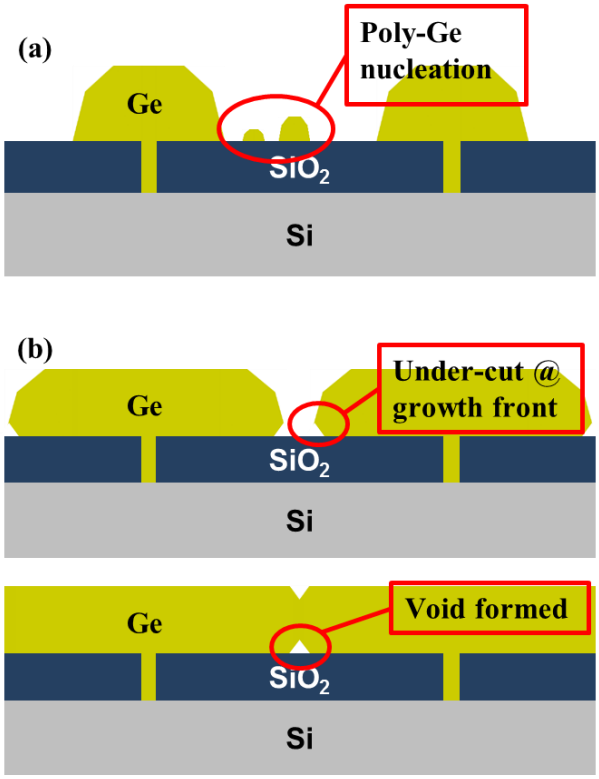

Figure 2.7. Issues with lateral overgrowth. (a) Poly-crystalline Ge nucleation. (b) Void formation.

2.2.2 Poly crystalline Ge nucleation

Poly-crystalline nucleation is caused because of the limited growth selectivity SiO_2 provides. During the Ge growth, SiO_2 does not provide stable sites for Ge adatoms. An incoming Ge species diffuses along the growth mask surface, after it is adsorbed on the surface. If the species reaches a nearby Ge epitaxial crystal within a surface diffusion length, they add to the epitaxial growth. But if partial pressure of GeH_2 during the growth

is too high, or the SiO_2 growth mask is wider than the diffusion length of Ge adatoms on SiO_2, poly-crystalline Ge nuclei form on SiO_2.

Thermally grown SiO_2, and low pressure chemical vapor deposition (LPCVD) SiO_2 and silicon nitride (Si_3N_4) were tried as the growth masks. Similar to selective growth of Si [21], Si_3N_4 is found to provide poor growth selectivity to Ge. LPCVD SiO_2 also provides limited growth selectivity, but high temperature (higher than 1000 ℃) densification greatly improves the growth selectivity. Thermal SiO_2 grown at temperature higher than 1000 ℃ provides high growth selectivity.

Even with the high temperature thermal oxide grown at 1100 ℃, poly crystalline Ge nuclei are formed on SiO_2 surfaces during relatively thick Ge growth required for lateral overgrowth. Similar to the lateral overgrowth of Si using SiO_2 as a growth mask [22], adding an etchant gas (HCl) very effectively suppress the nucleation (Figure 2.8. (a) and Table 2.1). For comparison, selective growth of Ge is done with different HCl gas flow during the Ge growth. 300 nm thermal SiO_2 grown at 1100 ℃ is used as a growth mask. Growth window width is fixed to 500 nm, and the growth mask width to 5 μm. During the growth, GeH_4 flow is fixed to 40 sccm, and the HCl flow is varied from 0 sccm to 160 sccm. When the 5 μm wide SiO_2 growth mask is covered by the lateral overgrowth, the nuclei density is counted at ~50 μm away from the growth opening. With 160 sccm of HCl, the actual nuclei density within the active GOI region between growth windows is effectively eliminated (Figure 2.8. (b)).

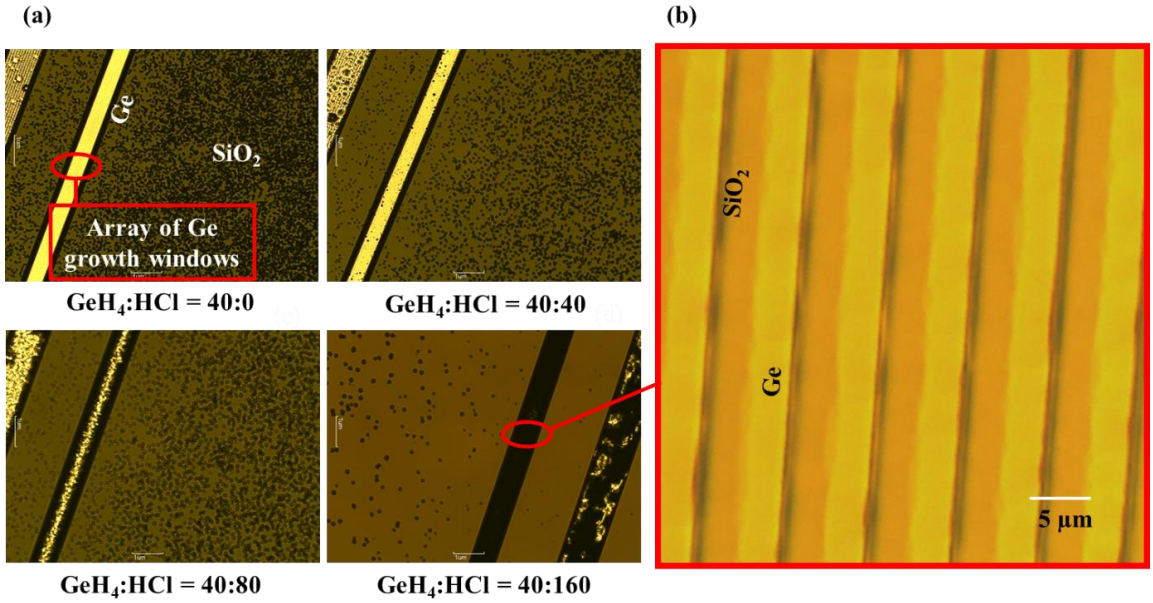

Figure 2.8. Nucleation suppression by HCl. (a) Nucleation with varying HCl flow (copyright 2013 IEEE) [12]. (b) Nucleation suppression on SiO_2 between growth windows. Growth is done at 600 ^oC and 30 Torr.

GeH_4 (sccm)	HCl (sccm)	Nucleation density (/ 100 μm^2)
40	0	> 100
40	40	35
40	80	25
40	160	5

Table 2.1. Nuclei density with varying HCl flow. Reprinted with permission [18]. Copyright 2015 Elsevier.

2.2.3 Void elimination

During the lateral growth, <311>, <111>, and <001> facets typically appear. And at the growth front of a growing Ge crystal, negative sloped growth undercuts are formed (Figure 2.9). Due to the undercut at the growth fronts during the lateral overgrowth, a void is formed at the center of the GOI region. To eliminate the void, formation of the typical facets and the undercut at the growth fronts need to be studied and understood.

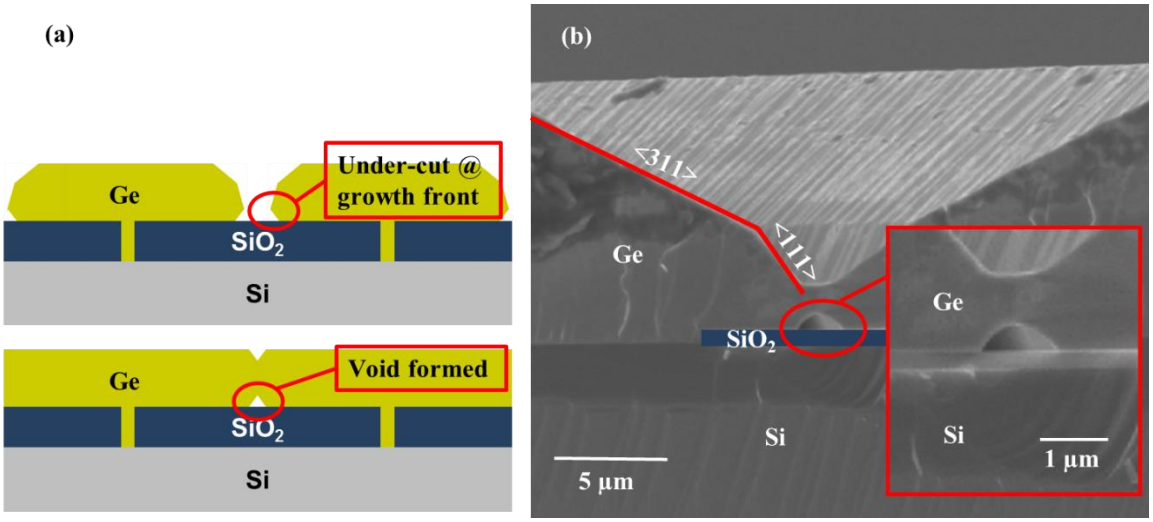

Figure 2.9. Void formation in GOI. (a) Undercut at the growth point and void formation. (b) Void and crystal facets. Growth done at 600 ºC and 30 T.

2.2.3.1 Growth kinetics

What determines facet growth during the growth? Growth rate of each facet is determined by three fluxes: i) Ge adatom coming from the environment (J), ii) Ge adatom surface diffusion from a neighboring facet (I_{in}), and iii) Ge adatom diffusion to the next

facet (I_{out}). (Figure 2.10. (a)). During the lateral overgrowth (Figure 2.10. (b)), since Ge does not grow well on a SiO_2 surface, there is a net flux of Ge adatoms from SiO_2 growth mask towards growing Ge crystals. As a result, on the same <001> facet at the top of the Ge crystal, <001> facet closer to the SiO_2 growth window becomes higher (Figure 2.11. (a)). Since Ge facets facing the SiO_2 growth mask typically exhibit faster growth, the crystal tends to shift towards SiO_2 growth mask area (Figure 2.11. (b)).

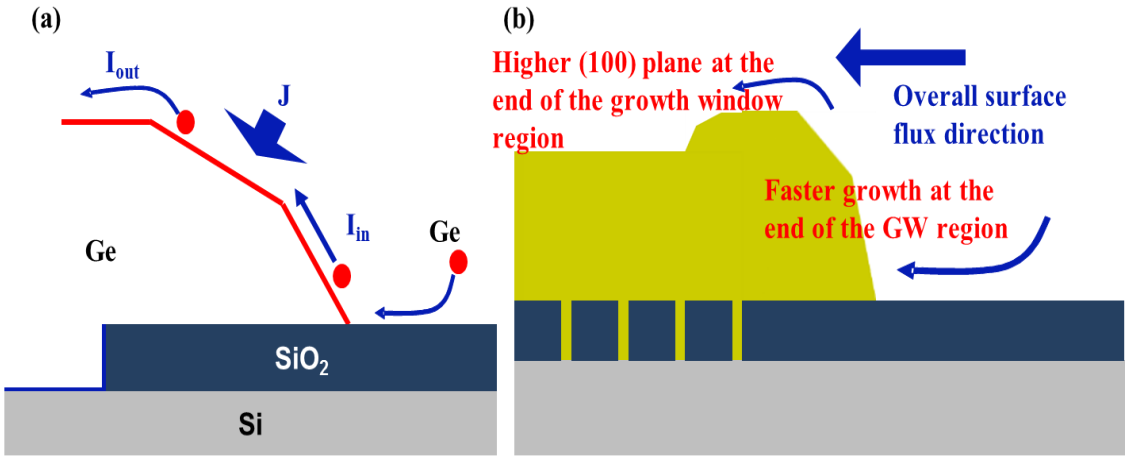

Figure 2.10. Ge facet growth. (a) Ge adatom fluxes, and (b) Ge growth during lateral overgrowth.

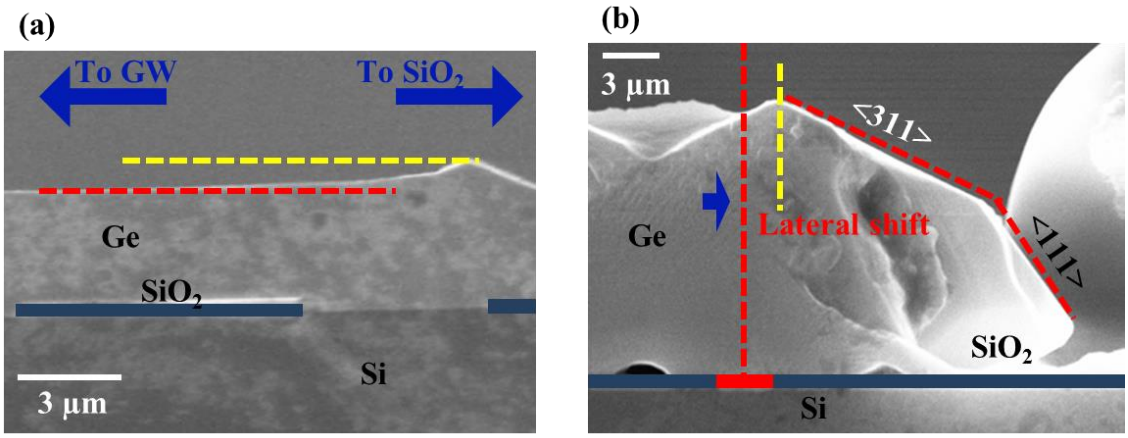

Figure 2.11. Ge facet growth during lateral overgrowth. (a) <001> facet height difference. (b) Shift of Ge crystal towards SiO_2 growth mask.

Now, let us consider how the facets are formed in the beginning of the growth. After deposition of the fist monolayer, for the second monolayer deposition, three lattice sides close to SiO_2 growth mask (marked as blue in Figure 2.12. (a)) cannot be occupied by Ge, due to the high interface energy between Ge and SiO_2. If the sites are occupied by Ge atoms, Ge atoms have to make contact to SiO_2 sidewall, increasing the energy of the system. Now, the lattice site marked as green in Figure 2.12. (a) determines the facet formation. If occupying the site is energetically more stable, and the crystal grows following the model illustrated in Figure 2.12. (b), <311> facet is formed. If the site is kept empty, and the crystal grows as illustrated in Figure 2.12. (c), <111> facet is formed [23]. For Ge, considering the surface reconstruction energies, model in Figure 2.12. (b) is energetically more stable. As a result, at the beginning of the selective growth process, <311> facet is formed. After the <311> facet is formed, in the beginning, Ge adatoms

arriving on or diffusing in the facet will diffuse up to the <001> facet, and <311> facet extends. But when the length of the <311> facet becomes longer than the diffusion length of Ge adatoms on the facet, <311> facet also grows. When the <311> facet grows, again, to avoid forming high energy interface between Ge and SiO_2 sidewall, <111> facet with higher angle is formed (Figure 2. 13. (c)) [24]. Once length of the <111> facet grows longer than the diffusion length, the <111> facet also grows, and the Ge crystal eventually fills the growth window completely. As a result, when the Ge growth window is filled and the lateral growth starts, Ge crystal is usually surrounded by <111>, <311>, and <001> facets (Figure 2.13. (d)).

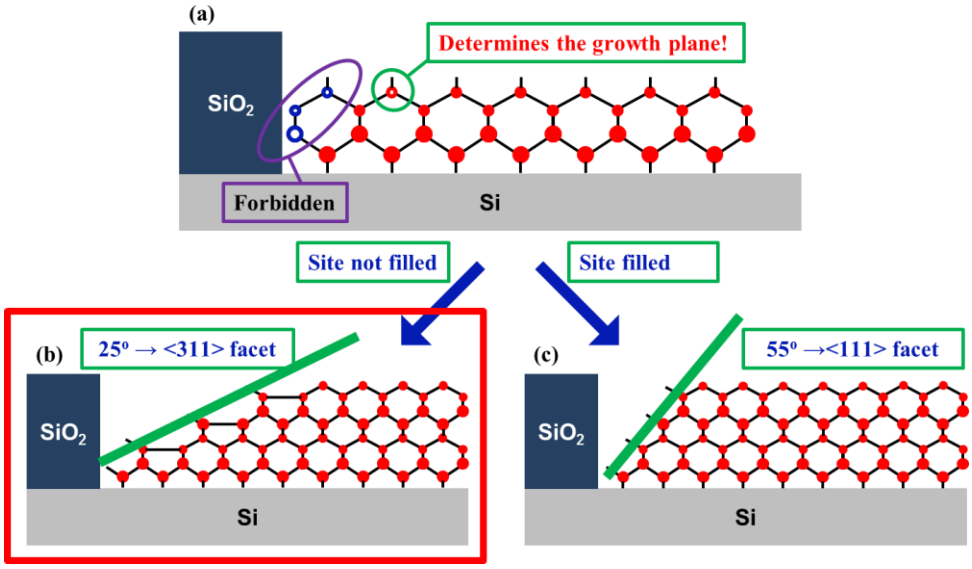

Figure 2.12. Facet formation during the selective growth of Ge on Si.

Up to the point when Ge fills up the growth window, there is no sign of the undercut at the growth front or void formation (Figure 2.13. (d)). But when the lateral growth starts,

the undercuts are formed. That is because of the high interface energy between SiO_2 and Ge. The interface energy is minimized by forming the undercut (Figure 2.14). In this stage, Ge adatoms diffusing into the undercut diffuse up to the next facet, and the length of the undercut increases (Figure 2.14. (a)). Like facet formation and evolution during the selective growth (Figure 2.12), when the length of the undercut becomes longer than the Ge adatom diffusion length on the undercut, Ge grows on the undercut surface (Figure 2.13. (b)), and the size of the undercut does not grown further (Figure 2.14. (b)). Accordingly, when neighboring Ge crystals coalesce and void is formed, size of the void becomes independent of the width of the SiO_2 growth mask (Figure 2.15). From this observation, it can be concluded that the size of the void is determined by the Ge adatom diffusion length and growth rate of the facet at the growth front. If growth rate of the facet at the growth front is slow, and Ge adatom diffusion in the undercut is limited, undercut length would be minimized.

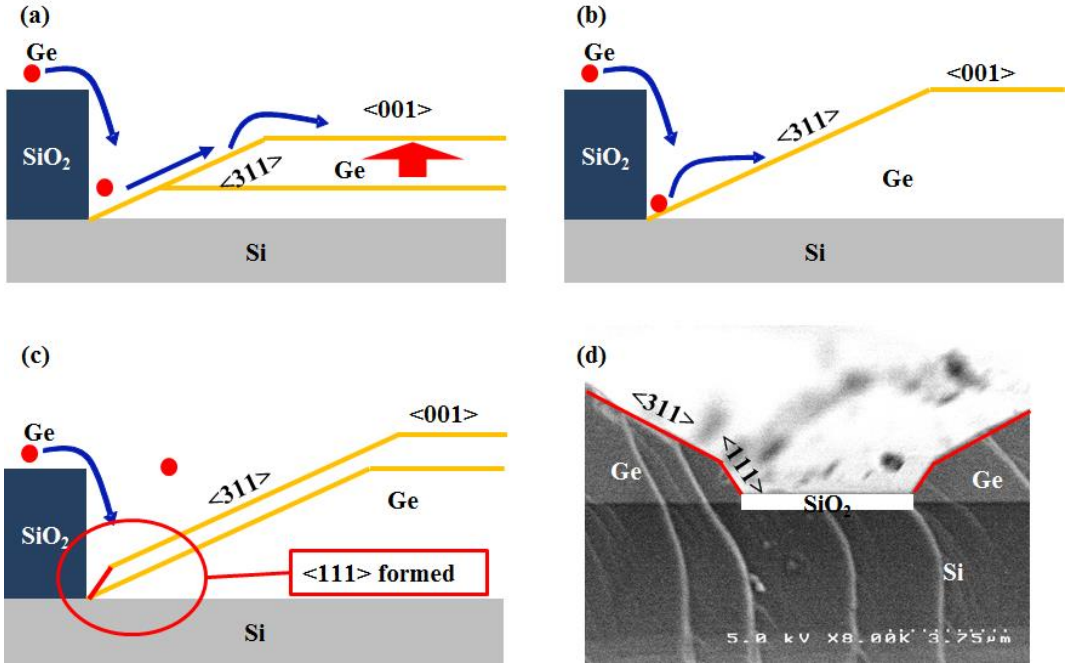

Figure 2.13. Facet formation and evolution. (a) <311> facet formation and adatom diffusion to <001> facet. (b) <311> facet growth when the facet length grows longer than Ge adatom diffusion length on <311> facet. (c) <111> facet formation. (d) Cross-sectional SEM iamge after the selective growth. Growth done at 600 ^{o}C, 30 T.

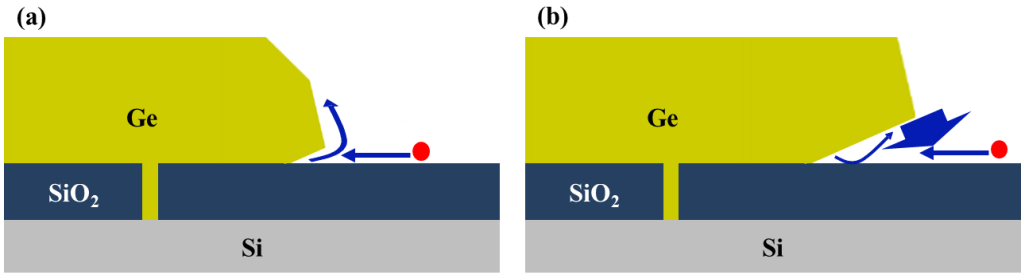

Figure 2.14. Undercut formation at the growth front during lateral overgrowth. (a) Undercut is formed due to the high interface energy. (b) Undercut growth when the length of the undercut becomes longer than the surface diffusion length.

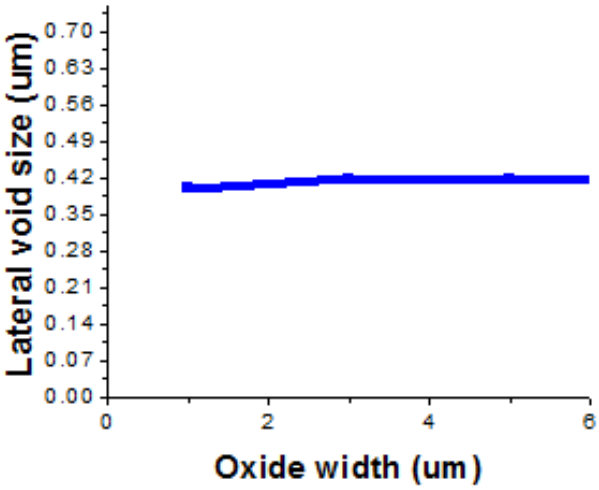

Figure 2.15. Lateral void size vs. SiO_2 growth window width. Growth is done at 600 ^oC, 30 Torr, with 40 sccm of GeH_4 and 40 sccm of HCl. Growth window width is fixed to 3 μm.

2.2.3.2 Void elimination

So far, growth kinetics and models are discussed to understand the formation of the facets, the undercuts, and the void. To eliminate the voids, two approaches are tried: 1) changing the interface energy between the insulator layer and Ge, and 2) by changing the growth condition to engineer the facet growth rates and surface diffusion of Ge adatoms in the undercut.

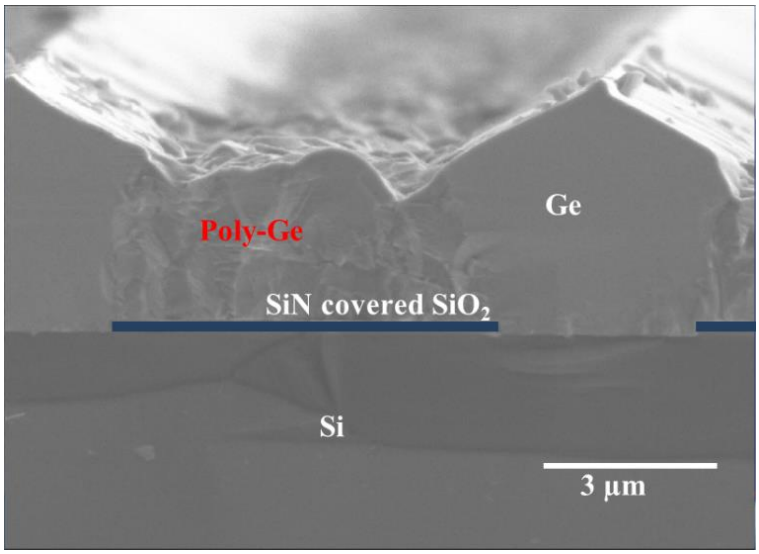

Figure 2.16. Lateral overgrowth with SiN covered SiO_2 as growth mask. Growth is done at 600 ^{o}C, 30 T.

During the lateral growth, undercut is formed due to the high interface energy between SiO_2 and Ge. The undercut could be altered by changing the interface energy. To achieve this, SiO_2 growth mask covered by a thin SiN layer is tried (Figure 2.16). But if the interface energy between the insulator and Ge is lowered, growth selectivity is also degraded, and poly-Ge nucleation grow from the interface surface. This cannot be used for GOI device applications.

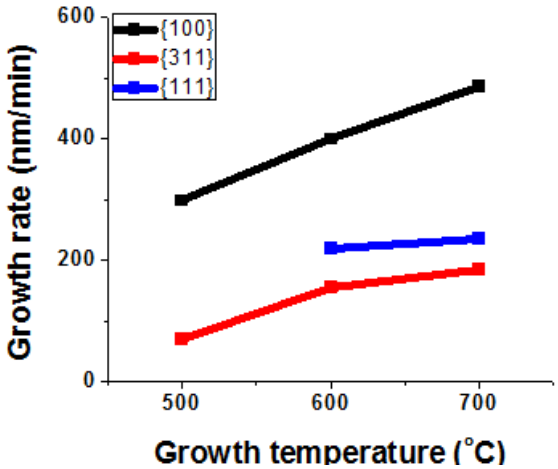

Figure 2.17. Facet growth rates vs. growth temperature. Growth is done at 30 Torr. Growth window width is fixed to 3 µm.

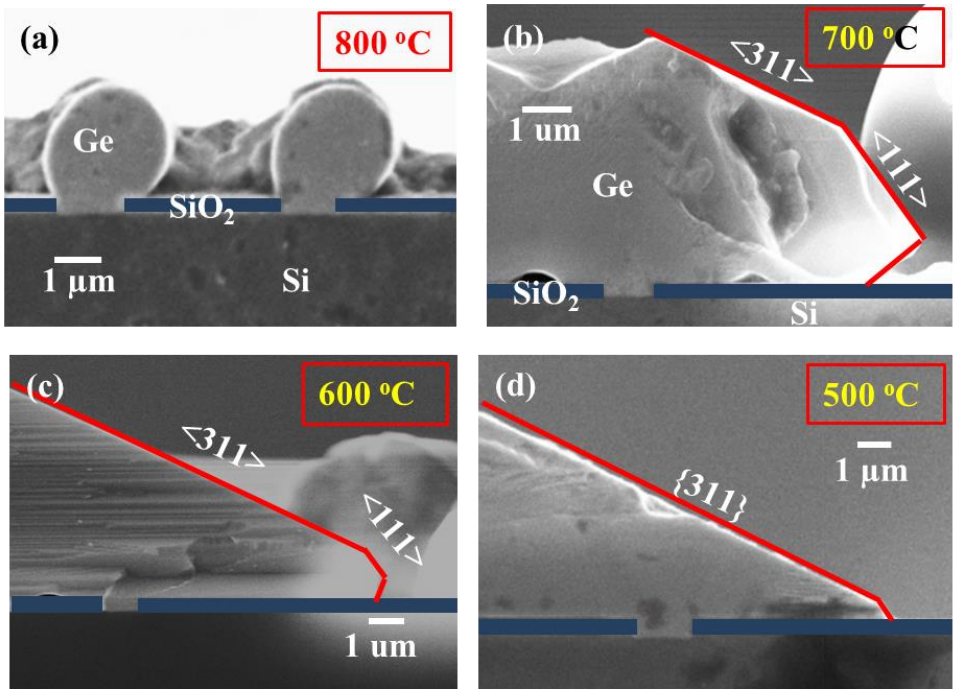

Figure 2.18. Ge crystal shape with different growth temperature. Growth pressure is fixed to 30 Torr.

By changing the growth conditions, relative growth rate of each facets and surface diffusion length of Ge adatoms are changed, and void size can be engineered. Dropping the growth temperature from 800 ºC to 500 ºC makes relative growth rate of <311> facet slower compared to other dominating facets (Figure 2.17), and <311> facet becomes dominant (Figure 2.18). At the same time, dropping the growth temperature also limits the surface diffusion of Ge adatoms, and the size of the undercut decreases. At 500 ºC, the undercut is finally eliminated (Figure 2.18. (d)), and as a result, when lateral overgrowth is complete and GOI is formed, eliminating the voids (Figure 2.19).

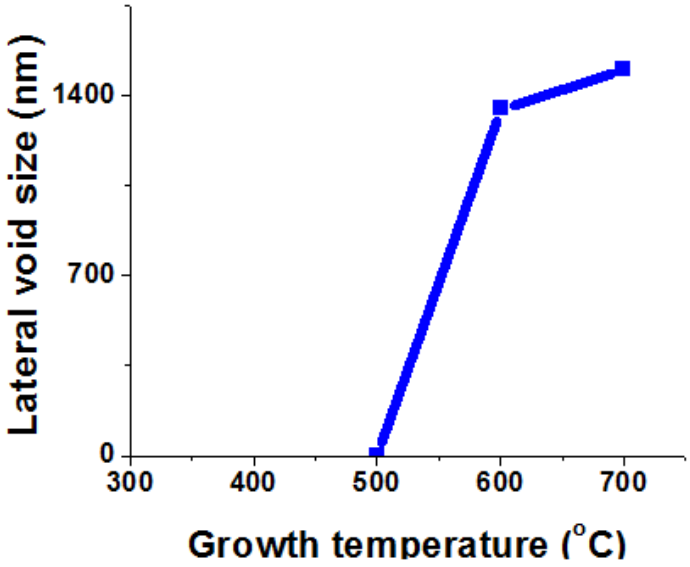

Figure 2.19. Lateral void size vs. growth temperature. At 500 ºC, void is eliminated. Growth is done at 30 Torr.

2.3 Lateral overgrowth for high quality void-less GOI

Previously in this chapter, techniques to suppress poly-crystalline Ge nucleation and elimination of voids are discussed. For high performance GOI device applications, it is crucial to achieve void-less GOI, without poly-crystalline Ge nucleation. When HCl gas is used to suppress nucleation, HCl etches different facets with different rate, and changes relative growth rate of each facets. At the same time, HCl also diffuse along the SiO_2 surface, and etches the growth front and the undercut region faster. As a result, when HCl is flown, undercuts and voids re-appear. It is difficult to achieve void-less GOI, without poly-crystalline Ge nucleation, using a single growth condition.

Void-less lateral overgrowth GOI without poly-crystalline nucleation is achieved by separating the growth into multiple steps, and carefully choosing growth conditions for each phase.

For the lateral overgrowth, to benefit from ART, width of the growth window is set to 0.5 μm, and the oxide thickness to 900 nm. Width of the SiO_2 growth mask is set to 5 μm. Growth windows are aligned to <110> direction on (001) Si substrate.

The first step is the Ge seed layer deposition. For better step coverage, 100 nm seed layer deposition is done at a lower temperature of 400 ^oC, followed by a hydrogen annealing at 825 ^oC. The cycle is repeated twice (Figure 2.20. (a) (i)). After the seed layer deposition, Ge is grown selectively with high flow of HCl, to maximize the growth selectivity and suppress poly-crystalline Ge nucleation. For better Ge crystal quality, growth temperature is raised to 600 ^oC. 160 sccm of HCl is used with 40 sccm of GeH_4 (Figure 2.20. (a) (ii)). After the Ge crystals completely fill the growth windows, lateral

growth is done at a condition which eliminates the undercut and the void. Growth temperature is set to 500 ^{o}C, with no HCl (Figure 2.20. (a) (ii)). After the coalescence, <001> facet growth becomes dominating and valleys are filled. For higher crystal quality and faster growth, growth temperature is raised back to 600 ^{o}C. At this stage, no poly-crystalline nucleation can happen in the GOI region, so no HCl is used. The surface of the GOI is planarized and the thickness is controlled by CMP (Figure 2.20. (b)).

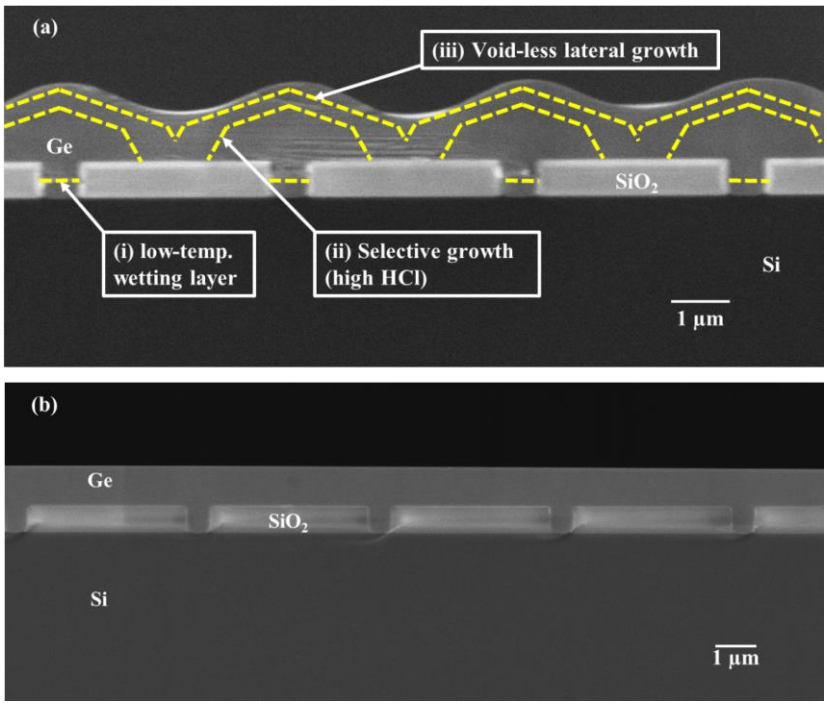

Figure 2.20. Lateral overgrowth for GOI. (a) Dashed yellow lines show successive stages of growth. (i) Low temperature seed layer growth at 400 ^{o}C. (ii) Selective growth with high HCl flow. Growth is done at 600 ^{o}C, with 40 sccm of GeH_4 and 160 sccm of HCl. (iii) Lateral growth without undercut and void. Growth is done at 500 ^{o}C with no HCl. (b) lateral overgrowth GOI after CMP.

2.4 Characterization of GOI

Cross-sectional transmission electron microscopy (TEM) (Figure 2.21) confirms high crystal quality single crystalline GOI is achieved by the lateral overgrowth process (Figure 2.20).

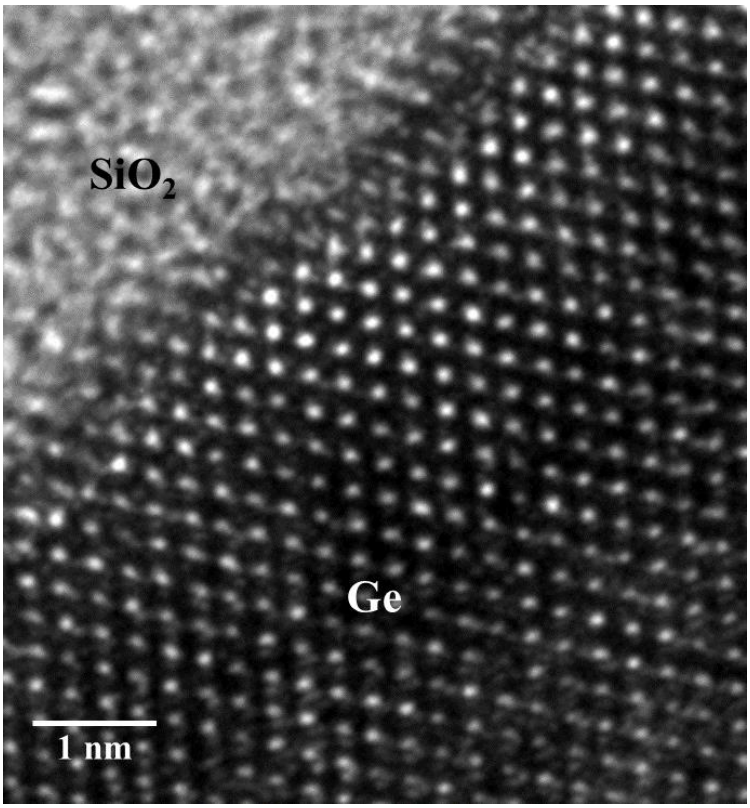

Figure 2.21. Cross-sectional TEM on the lateral overgrowth GOI.

Plan-view TEM is used to count the TDD in the GOI (Figure 2.22). After the lateral overgrowth and CMP to form the GOI, the sample is polished from the backside Si substrate leaving only the thin GOI layer. Based on the TEM images of the polished sample, TDD is counted. Ge in the GOI region, on the SiO_2, exhibits low TDD of 1-

3×10^6 /cm^2, while Ge within the growth window shows higher number of 10^8 /cm^2. The two orders of magnitude difference between the two regions prove the defect limiting mechanisms, ART and defect necking, very effectively confine the threading dislocations within the growth window region, drastically enhancing the crystal quality of the GOI.

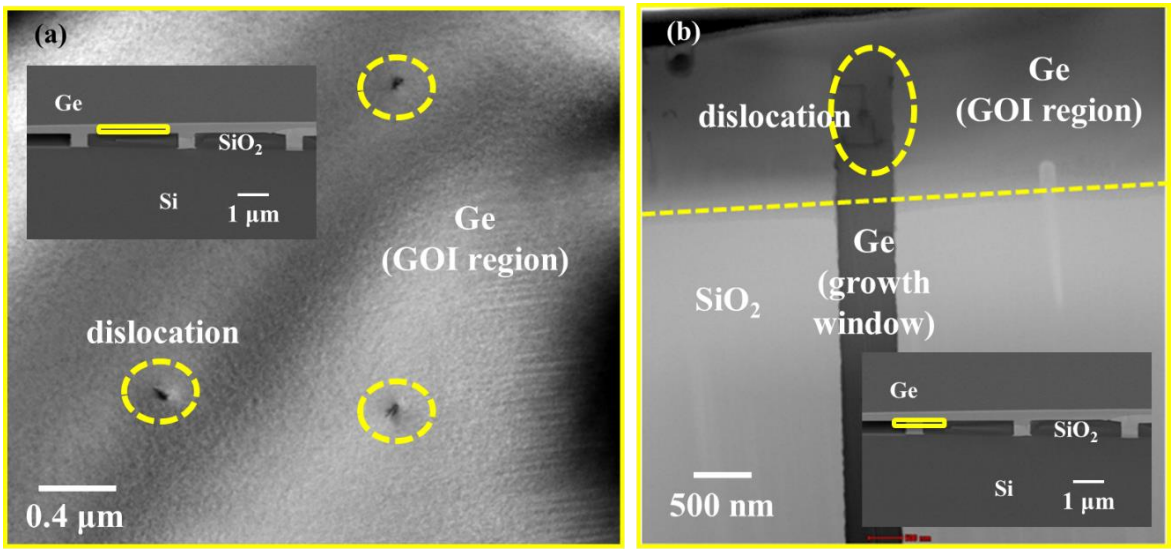

Figure 2.22. Plan-view TEM on the lateral overgrowth GOI. (a) In the GOI region, on SiO_2. (b) In the growth window.

Minority carrier lifetime in the GOI region is measured by time-resolved photoluminescence (TRPL) measurement. The GOI sample is illuminated by laser to excite carriers, and the photoluminescence increases accordingly. At time 0, laser is turned off. As photo generated carriers recombine, the minority carrier density decays, and the photoluminescence signal as well. From the decaying photoluminescence signal, minority carrier lifetime can be extracted. Minority carrier lifetime on a 600 nm lateral overgrowth GOI and 600 nm Ge directly grown on Si are measured and compared. The

extracted results are shown in Figure 2.23 and Table 2.2. Due to the higher crystal quality with low TDD, and due to the absence of the defective Si/Ge interface beneath the Ge layer, lateral overgrowth GOI shows 7.4 times longer minority carrier lifetime.

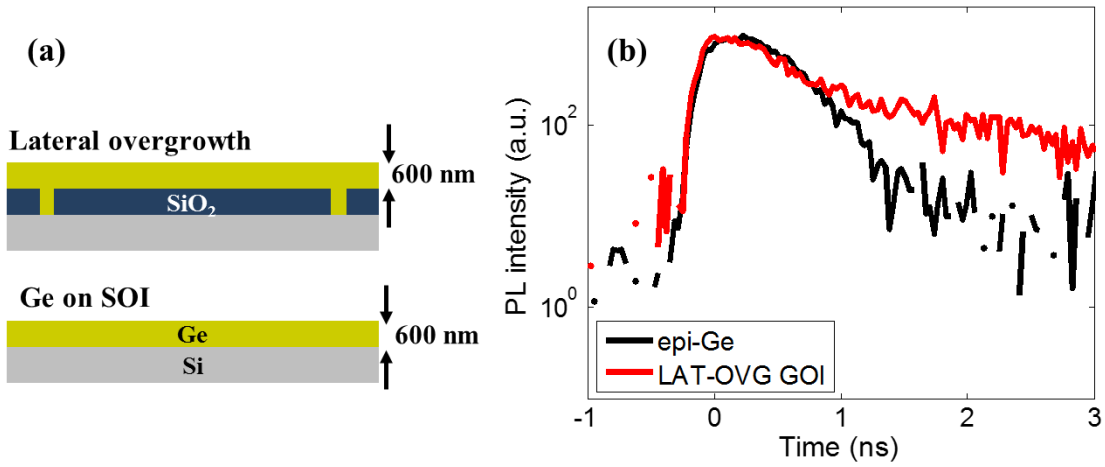

Figure 2.23. Time resolved photoluminescence measurement on lateral overgrowth GOI and Ge grown on Si. (a) Sample structures and (b) photoluminescence signal decay over time [18].

	600 nm epi Ge (Bulk growth)	Lateral overgrowth GOI
TDD (/cm^2)	3×10^8	$1\text{-}3\times10^6$
Lifetime (ns)	0.478	3.534

Table 2.2. Minority carrier lifetime measured by time resolved photoluminescence measurement.

Photoluminescence intensity from a 600 nm thick lateral overgrowth GOI and 600 nm Ge directly grown on 20 nm SOI with 400 nm SiO_2 box are compared (Figure 2.24). Again, due to the higher crystal quality and the absence of the defective interface layer, higher photoluminescence signal is observed from the lateral overgrowth GOI.

For device applications, residual strain in the Ge film plays an important role. Especially for optical devices, residual strain in Ge grown on Si extends the absorption edge of Ge to cover the entire C-band telecommunication wavelength [25]. Higher tensile strain further shifts the absorption edge and enhances absorption. Based on a COMSOL^{TM} Multiphysics package calculation, compared to a same thickness Ge grown on SOI, lateral overgrowth GOI is expected to show higher level of residual tensile strain (Figure 2.25). By Raman spectroscopy, strain in a 500 nm thick lateral overgrowth GOI with 950 nm SiO_2 and 500 nm thickness Ge growth on 20 nm SOI with 400 nm SiO_2 box is measured and compared (Table 2.3). As predicted from the calculation, lateral overgrowth GOI shows higher tensile strain.

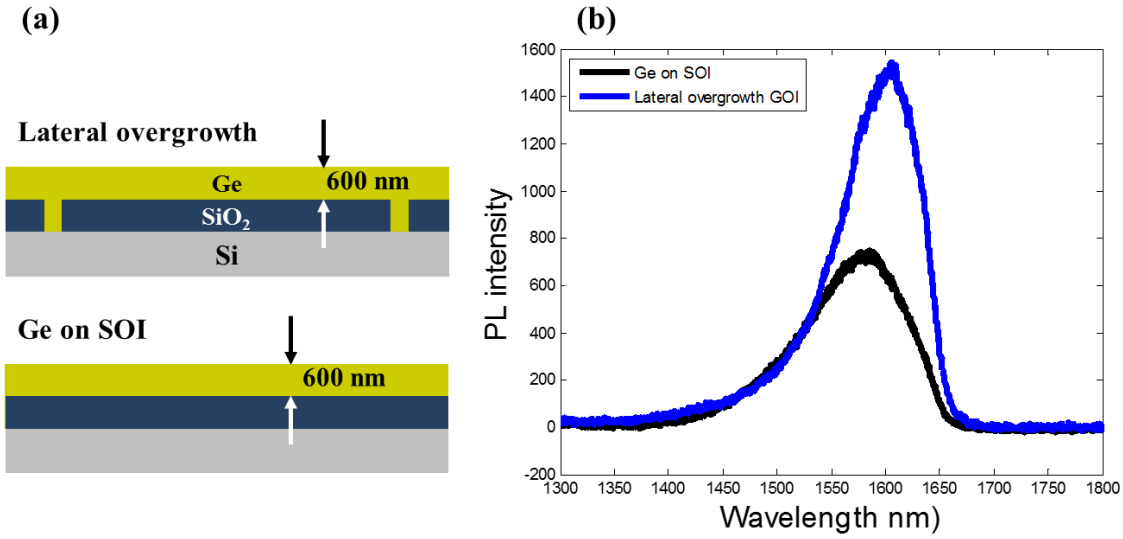

Figure 2.24. Photoluminescence signal comparison on lateral overgrowth GOI and Ge grown on thin SOI. (a) Sample structures. (b) Photoluminescence signal [26].

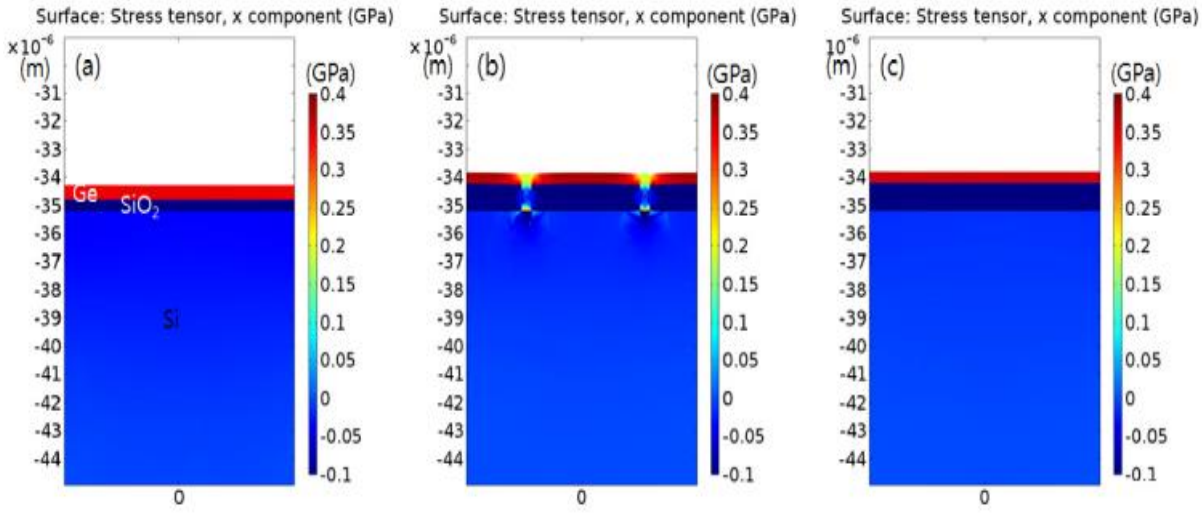

Figure 2.25. Residual strain calculation on (a) 500 nm Ge grown on 20 nm SOI with 400 nm SiO_2, (b) 500 nm lateral overgrowth GOI on 950 nm SiO_2, and (c) 500 nm Ge grown on 20 nm SOI with 950 nm SOI [26].

Raman measurement	Ge wafer	Lateral overgrowth	Ge on SOI
Peak position (/cm)	300.160	299.292	299.346
Tensile strain (%)	-	0.209 %	0.196

Table 2.3. Residual tensile strain on 500 nm lateral overgrowth GOI with 950 nm SiO_2 and 500 nm Ge grown on 20 nm SOI with 400 nm SiO_2 box [26].

2.5 Further application to germanium on "nothing"

High strain Ge optical applications require high crystal quality Ge on "nothing" (GON) suspended membranes [27-28]. After the lateral overgrowth for GOI and CMP, by selectively removing the SiO_2 growth mask by wet etching, monolithically integrated high crystal quality GON on Si can be achieved.

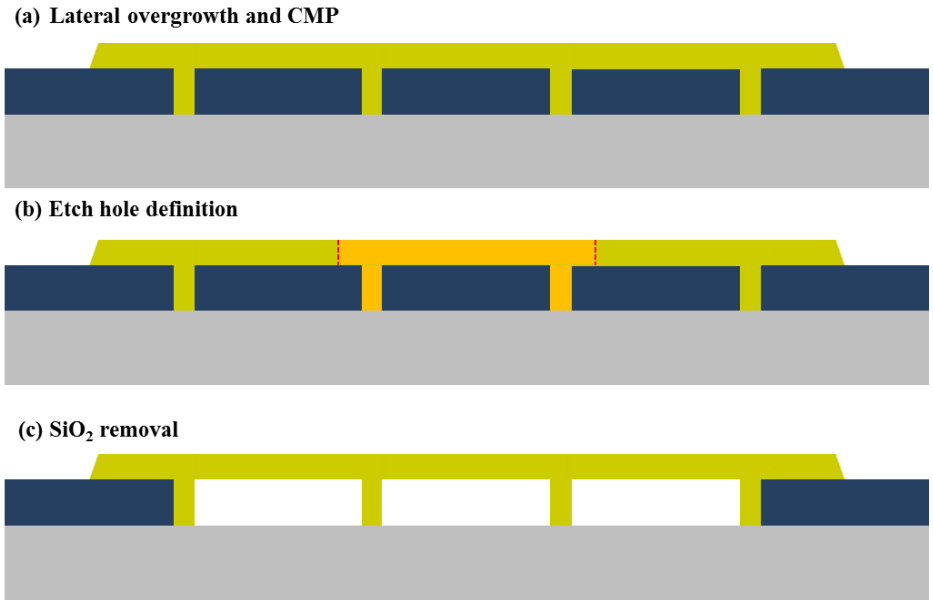

Figure 2.26. Wet etching of SiO_2 for GON. (a) Lateral overgrowth GOI after CMP. (b) Etch hole definition by optical lithography and dry etching. (c) Wet etching of SiO_2 using 6:1 BOE.

Figure 2.26 shows the schematic process flow for the GON membrane. On the polished surface of lateral overgrowth GOI after CMP (Figure 2.26. (a)), etch holes are defined by optical lithography and dry etching, to ensure faster lateral wet etching (Figure 2.26. (b)). Through the etching holes, SiO_2 is wet etched by 6:1 buffered oxide etch (BOE) (Figure 2.26. (c)). Figure 2.27 shows SEM images of the resulting GON membrane.

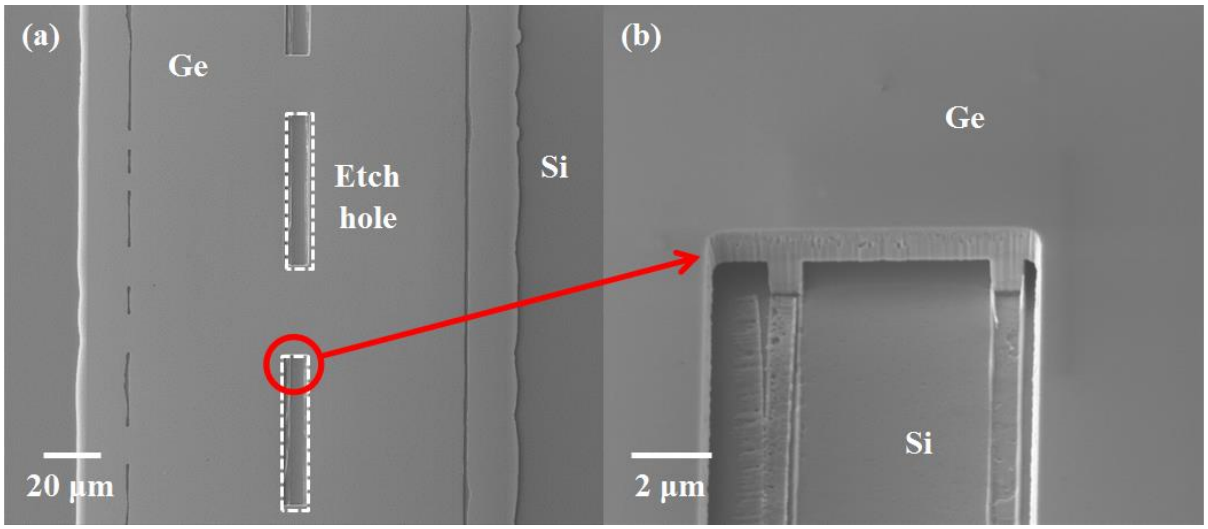

Figure 2.27. GON membrane on Si from lateral overgrowth and wet etching through etch holes.

Alternatively, GON membrane can be achieved by defining a mesa followed by the wet etching. Starting from the lateral overgrowth GOI (Figure 2.28. (a)), instead of defining etch holes, Ge mesa is defined by dry etching (Figure 2.28. (b)). SiO_2 growth mask is then removed by wet etching, using 6:1 BOE (Figure 2.28. (c)). The resulting GON membrane is shown in Figure 2.29.

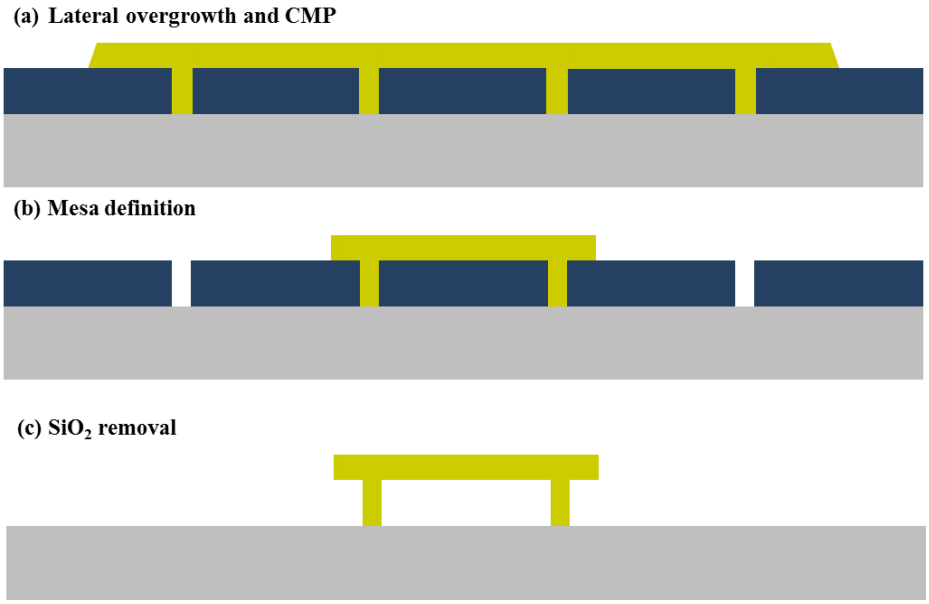

Figure 2.28. Wet etching of SiO_2 for GON. (a) Lateral overgrowth GOI after CMP. (b) Etch hole definition by optical lithography and dry etching. (c) Wet etching of SiO_2 using 6:1 BOE.

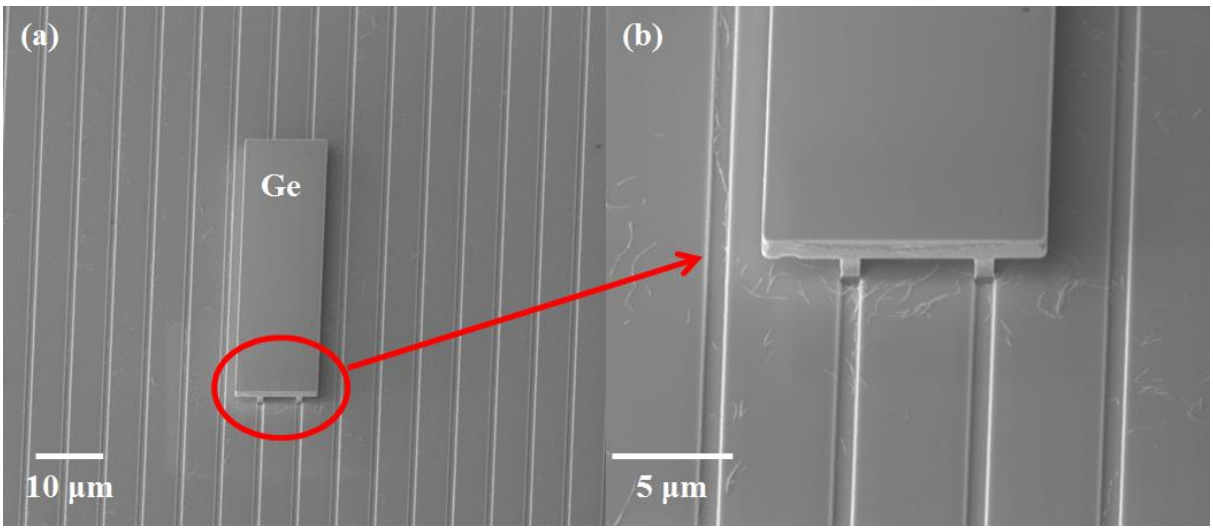

Figure 2.29. GON membrane on Si from lateral overgrowth and wet etching after mesa definition.

By using the GON from lateral overgrowth GOI, monolithic integration of highly strained Ge based optical device can be integrated on Si.

2.6 Conclusion

To achieve high crystal quality lateral overgrowth GOI without void, growth kinetics and growth models for the Ge growth are studied. The lateral overgrowth process is optimized, and void-less GOI is monolithically integrated on Si. The lateral overgrowth GOI shows high crystal quality with low TDD of $1\text{-}3\times10^{6}$, and ×7.4 times longer minority carrier lifetime compared to Ge directly grown on Si is observed. Lateral overgrowth GOI also shows higher residual tensile train than same thickness Ge grown on Si.

REFERENCE

[1] R. Hull and J. C. Bean, "Germanium silicon: physics and materials," Semiconductors and semimetals 56, Academic Press, 1999

[2] M. Carmody, D. Lee, M. Zandian, J. Phillips, and J. Arias, "Threading and misfit-dislocation motion in molecular-beam epitaxy-grown HgCdTe Epilayers," Journal of Electronic Materials 39 (7), 710-716 (2003)

[3] K. Varga, L. G. Wang, S. T. Pantelides, and Z. Zhang, "Critical layer thickness in Stranski-Krastanow growth of Ge on Si(001)," Surface Science 562, L225-L230 (2004)

[4] J. Halpin, "High quality relaxed germanium layers on silicon," MSc thesis, University of Warwick (2010)

[5] S.-J. Kahng, Y. Ha, J.-Y. Park, S. Kim, D. Moon, and Y. Kuk, "Hydrogen-surfactant mediated growth of Ge on Si(001)," Physical Review Letters 80 (22), 4931–4934 (1998)

[6] A. Nayfeh, C. O. Chui, K. C. Saraswat, and T. Yonehara, "Effects of hydrogen annealing on heteroepitaxial-Ge layers on Si: surface roughness and electrical quality," Applied Physics Letters 85, 2815 (2004)

[7] H.-Y. Yu, S.-L. Cheng, J.-H. Park, A. K. Okyay, M. Cengiz Onbasli, B. Ercan, Y. Nishi, and K. C. Saraswat, "High quality single-crystal germanium-on-insulator on bulk Si substrates based on multistep lateral over-growth with hydrogen annealing," Applied Physics Letters 97, 063503 (2010)

[8] L. Dong, J. Schnitker, R. W. Smith, and D. J. Srolovitz, “Stress relaxation and misfit dislocation nucleation in the growth of misfitting films: a molecular dynamics simulation study,” Journal of Applied Physics 83 (1), 217-227 (1998)

[9] J.-H. Yang, Y. Wei, X.-Y. Cai, and J.-Z. Ran, “The effects of threading dislocations and tensile strain in Ge/Si photodetector,” Microelectronics International 27 (2), 113-116, (2010)

[10] G. Wang, R. Loo, E. Simoen, L. Souriau, M. Caymax, M. M. Heyns, and B Blanpain, “A model of TDD in strain-relaxed Ge and GaAs epitaxial films on Si (100),” Applied Physics Letters 94, 102115 (2009)

[11] H.-Y. Yu, J.-H. Park, A. K. Okyay, and K. C. Saraswat, “Selective-area high-quality germanium growth for monolithic integrated optoelectronics,” IEEE Electron Device Letters 33 (4), 579-581 (2012)

[12] H.-Y. Yu, M. Kobayashi, J.-H. Park, Y. Nishi and K. C. Saraswat, “Novel germanium n-MOSFETs with raised source/drain on selectively grown Ge on Si for monolithic integration," IEEE Electron Dev. Lett. 32 (4), 446-448 (2011)

[13] H.-Y. Yu, M. Ishibashi, J.-H. Park, M. Kobayashi, and K. C. Saraswat, “p-Channel Ge MOSFET by selectively heteroepitaxially grown Ge on Si,” IEEE Electron Dev. Lett. 30 (6), 675-677 (2009)

[14] J.-S. Park, J. Bai, M. Curtin, B. Adekore, M. Carroll, and A. Lochefeld, “Defect reduction of selective Ge epitaxy in trenches on Si(001) substrates using aspect ratio trapping,” Applied Physics Letters 90, 052113 (2007)

[15] M. J. H. van Dal, G. Vellianitis, B. Duriez, G. Doornbos, C.-H. Hsieh, B.-H. Lee, K.-M. Yin, M. Passlack, C. H. Diaz, “Germanium p-channel FinFET fabricated by aspect ratio trapping,” IEEE Transactions on Electron Devices 61 (2), 430-436 (2014)

[16] H.-Y. Yu, S. Cheng, J.-H. Park, A. K. Okyay, M. Cengiz Onbali, B. Ercan, Y. Nishi, and K. C. Saraswat, “High quality single-crystal germanium-on-insulator on bulk Si substrates based on multistep lateral over-growth with hydrogen annealing,” Applied Physics Letters 97, 063503 (2010)

[17] J.-S. Park, M. Curtin, J. M. Mydrick, J. Bai, J.-T. Li, Z. Cheng, M. Carroll, J. G. Fiorenza, and A. Lochtefeld, “Low-defect-density Ge epitaxy on Si(001) using aspect ratio trapping and epitaxial lateral overgrowth,” Electrochemical and Solid-State Letters 12 (4), H142-H144 (2009)

[18] J. H. Nam, S. Alkis, D. Nam, F. Afshinmanesh, J. Shim, J.-H. Park, M. brongersma, A. K. Okyay, T. I. Kamins, and K. C. Saraswat, “Lateral overgrowth of germanium for monolithic integration of germanium-on-insulator on silicon,” Journal of Crystal Growth 416, 21-27 (2015)

[19] J. H. Nam, T. Fuse, Y. Nishi, and K. C. Saraswat, “Germanium on insulator (GOI) structure using hetero-epitaxial lateral overgrowth on silicon,” ECS Transactions 45 (4), 203-208 (2012)

[20] J. H. Nam, W. S. Jung, J. Shim, T. Ito, Y. Nishi, J.-H. Park, and K. C. Saraswat, “Germanium on insulator (GOI) structure locally grown on silicon using hetero

epitaxial lateral overgrowth," in 2013 IEEE SOI-3D Subthreshold Microelectronics Technology Unified Conference (S3S), 2013

[21] J. T. Fitch, "Selective mechanisms in low pressure selective epitaxial silicon growth," Journal of Electrochemical Society 141 (4), 1046-1055 (1994)

[22] D. R. Bradbury, T. I. Kamins, and C. -W. Tsao, "Control of lateral epitaxial chemical vapor deposition of silicon over insulators," Journal of Applied Physics 55 (2), 1984

[23] H. Hirayama, M. Hiroi, and T. Ide, "{311} facets of selectively grown epitaxial Si layers on SiO_2-patterned Si(100) surfaces," Physical Review B 48 (23), 17331-17337 (1993)

[24] S.-H. Lim, S. Song, G.-D. Lee, E. Yoon, and J.-H. Lee, "Facet evolution in selective epitaxial growth of Si by cold-wall ultrahigh vacuum chemical vapor deposition," Journal of Vacuum Science Technology B 22 (2), 1071-1023 (2004)

[25] A. K. Okyay, A. M. Nayfeh, K. C. Saraswat, N. Ozguven, A. Marshall, P. C. McIntyre, and T. Yonehara, "Strain enhanced high efficiency germanium photodetectors in the near infrared for integration with Si," 19th Annual Meeting of the IEEE Lasers and Electro-Optics Society, 2006, 460-461

[26] J. H. Nam, F. Afshinmanesh, D. Nam, W. S. Jung, T. I. Kamins, M. L. Brongersma, and K. C. Saraswat, "Monolithic integration of germanium-on-insulator p-i-n photodiode on silicon," Optics Express 13 (12), 15816-15823 (2015)

[27] D. Nam, D. S. Sukhdeo, S.-L. Cheng, A. Roy, K. C.-Yao Huang, M. Brongersma, Y. Nishi, and K. C. Saraswat, “Electroluminescence from strained germanium membranes and implications for an efficient Si-compatible laser," Applied Physics Letters 100, 131112 (2012)

[28] D. Nam, D. Sukhdeo, S.-L. Cheng, K. C.-Y. Huang, M. Brongersma, Y. Nishi, and K. C. Saraswat, “Demonstration of Electroluminescence from Strained Ge Membrane LED,” International Si-Ge Technology and Device Meeting (ISTDM), 2012, 98-99

Chapter 3:

Photodiode on lateral overgrowth GOI

For high bandwidth photodiode for optical interconnects, GOI based Ge photodiodes have been under active study. In this chapter, previous approaches are reviewed, and a photodiode monolithically integrated on Si substrate based on lateral overgrowth is demonstrated. The new photodiode shows excellent diode characteristics with high responsivity and low dark current.

3.1 GOI photodiodes

To detour the issues of miniaturized interconnects, i.e., high power consumption, low band width and RC delay, optical interconnects have been under active study. Si, by far the most prevalent semiconducting material of nowadays semiconductor industry, cannot interact with C-band optical signals at 1550 nm wavelength, due to its high optical bandgap. For Si compatible optical interconnect systems, Ge has been considered as one of the strongest candidates for the building material. Direct band gap of 0.8 eV is slightly

higher than what is required to absorb 1550 nm optical signals, but when grown on Si, Ge typically experiences 0.2 % biaxial tensile strain, and the optical bandgap is lowered to cover the entire C-band [1]. Unlike compound semiconductors, Ge is a group IV material as is Si, and can be easily integrated without anti-phase disorder. Also, Ge is a CMOS compatible material, already integrated in the CMOS process, especially for source/drain stressors and more recently, for high performance SiGe channels [2-3].

In addition to the advantages of Ge, GOI based optical devices provides higher bandwidth through carrier isolation [4]. Various approaches to monolithically integrate GOI photodiodes on Si have been tried, but the diode performance has been limited with high dark current and low on/off ratio due to high TDD and defective Si/Ge interface.

Ge and GOI based photodiodes integrated on Si have been demonstrated, using epitaxial growth of Ge on Si and SOI [5-8]. But in general, due to the lattice constant mismatch between Ge and Si, Ge grown directly on Si or SOI suffers from high threading dislocation density and defective Si/Ge interface [9]. Therefore, the resulting photodiodes suffer from high dark current and low on/off ratio.

In this chapter, a lateral overgrowth GOI based photodiode monolithically integrated on Si is demonstrated. The photodiode exhibits excellent diode characteristics with high on/off ratio, low dark current, and high optical response.

3.2 Photodiode integration

High quality GOI platform is monolithically integrated on Si (001) substrate by lateral overgrowth. Following the lateral overgrowth process discussed in Chapter 2, 500 nm GOI is integrated on 950 nm SiO_2.

On a Si (001) substrate, 950 nm SiO_2 is thermally grown at 1100 ℃. Growth windows are defined following <110> direction, by optical lithography and dry etching. For ART, growth window width is set to 0.5 μm. GOI region width is set to 5 μm (Figure 3.1. (a)). For smoother starting Si surface for the growth, the last 50 nm of the etching is done by wet etching, using 20:1 HF. Immediately after photoresist removal and HF-last RCA cleaning, the sample is loaded into Applied Materials epi Centura reactor. Ge growth is done following the growth recipe discussed in Chapter 2. H_2 bake at 1000 ℃ removes any residual SiO_2 inside the growth window. Growth surface is prepared by a thin selective Si growth using DCS at 700 ℃. 300 nm thick Ge seed layer is selectively grown at 400 ℃ using GeH_4. On the seed layer, selective Ge growth is done at 600 ℃, with HCl to suppress polycrystalline Ge nucleation on SiO_2. When the growth windows are filled, lateral growth is continued at 500 ℃, for void-less GOI (Figure 3.1. (b)). When Ge crystals coalesces and GOI is formed, CMP is done to control the GOI thickness to 500 nm (Figure 3.1. (c)) [10-12].

To define the device region, 5 μm wide Ge mesa is defined by optical lithography and dry etching on the lateral overgrowth GOI (Figure 3.1. (d)). On the mesa, by optical lithography and ion implantation, 4 μm wide and 2 μm long n- and p- regions are defined, separated by 1 μm i-regions. 10^{14} /cm^2 phosphorus implanted at 50 keV and 10^{14} /cm^2

boron implanted at 20 keV are used for n- and p-type regions, respectively. The dopants are activated by 500 ^{o}C rapid thermal annealing (RTA) in a nitrogen ambient (Figure 3.1. (e)). Each photodiode has three n-type fingers, two p-type fingers, and i-regions in between. After defining the n- and p- regions, the device surface is passivated by 20 nm atomic layer deposition (ALD) aluminum oxide (Al_2O_3) and 20 nm low temperature CVD oxide (LTO). Metal contact vias are defined by optical lithography and wet etching using 20:1 buffered oxide etch (BOE), and a 20 nm titanium (Ti) / 180 nmm aluminum (Al) metal stack is used for the contacts. No anti reflection coating (ARC) is used. No additional forming gas anneal (FGA) is done. Figure 3.2 shows optical microscope images of the photodiode.

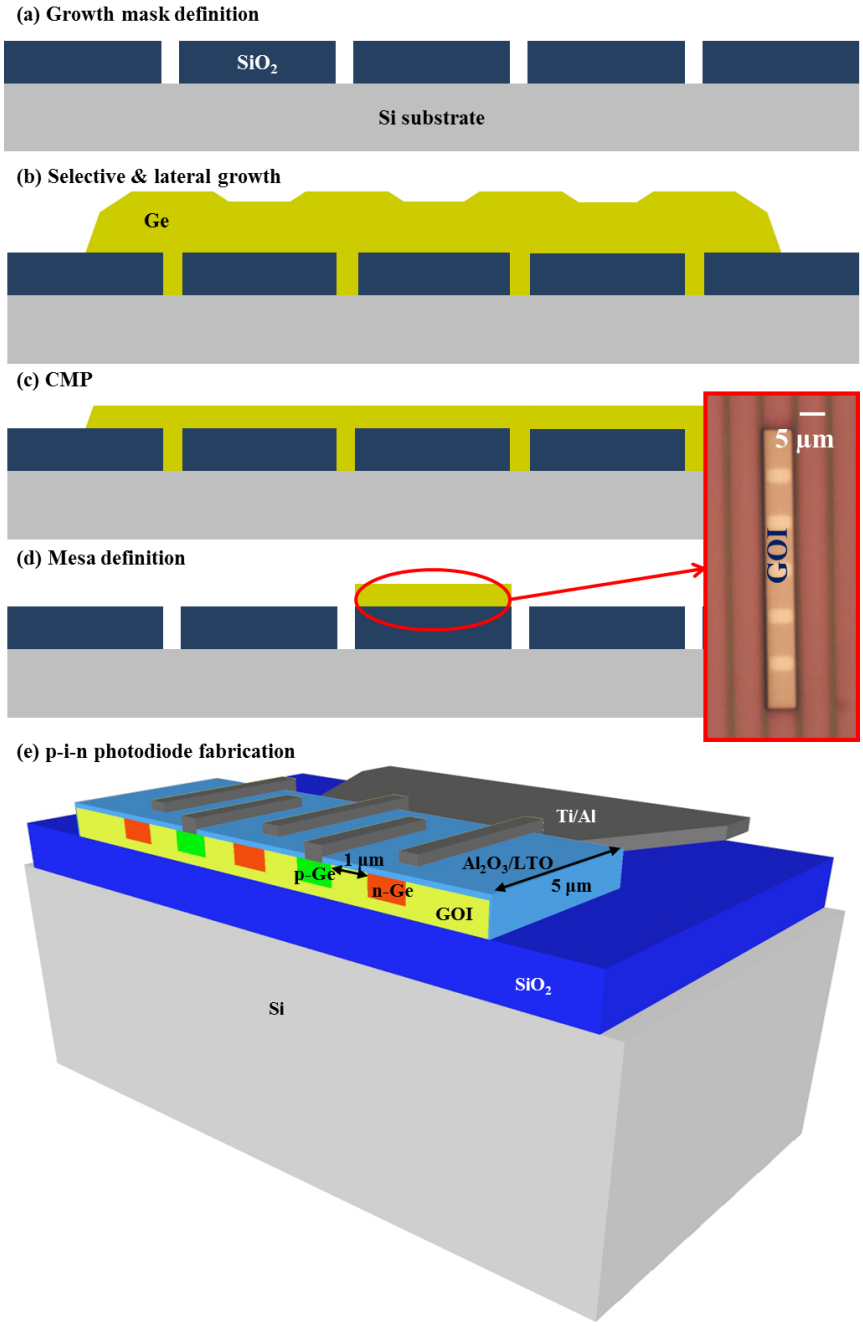

Figure 3.1. Lateral p-i-n photodiode fabrication. (a) SiO_2 thermal growth and growth window definition. (b) Lateral overgrowth of Ge for GOI. (c) CMP for surface planarization. (d) Mesa formation in the GOI layer. (e) Photodiode fabrication on GOI.

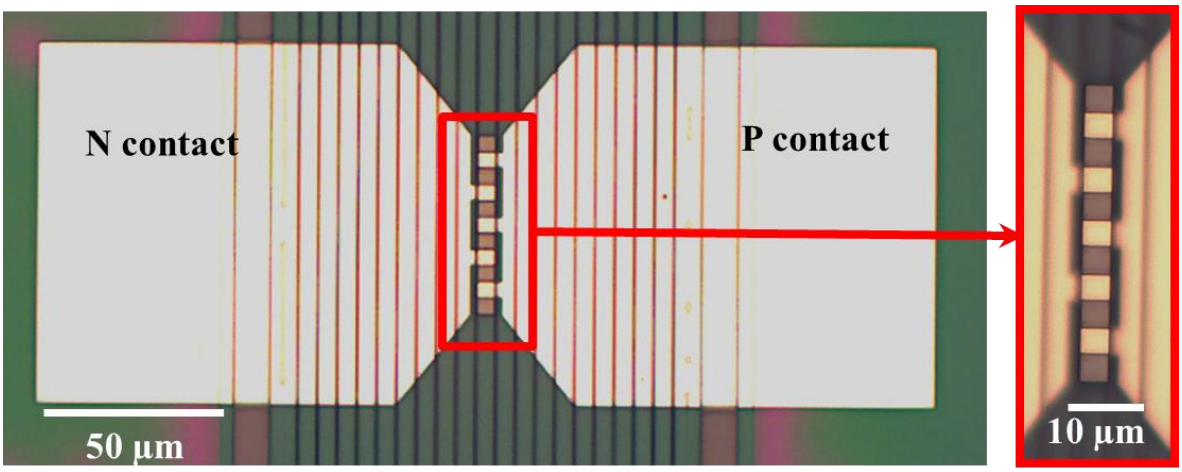

Figure 3.2. Lateral p-i-n photodiode on the lateral overgrowth GOI mesa [13].

3.3 Diode characterization

As discussed in Chapter 2, the resulting 500 nm thick lateral overgrowth GOI shows 1-3×10^6 /cm^2 of TDD, which is much lower than same thickness Ge grown on SOI (~10^8 /cm^2)

Figure 3.3 shows the diode current-voltage characteristics [13]. Also, lateral overgrowth separates the defective Si/Ge interface away from the GOI device region. The photodiode demonstrates excellent current-voltage characteristics with low dark current (~30 nA) and high on/off ratio of 6×10^4.

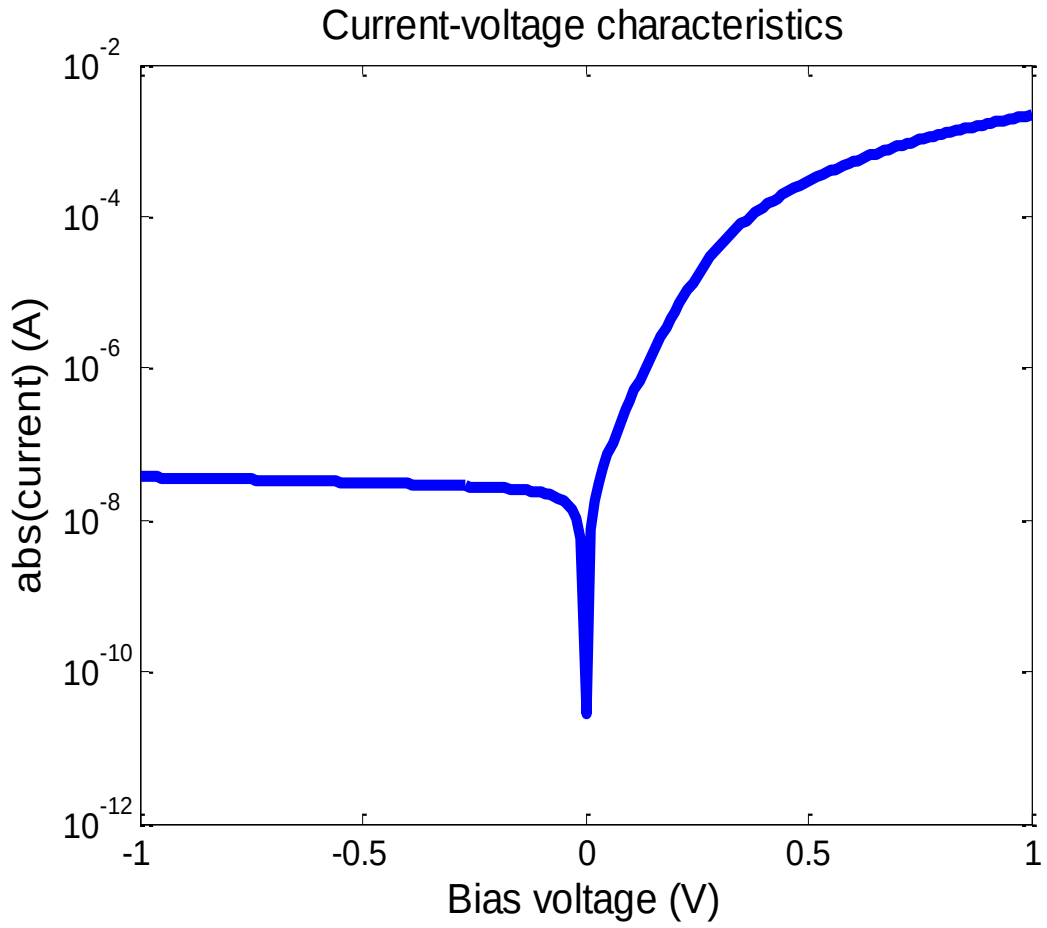

Figure 3.3. Diode current-voltage characteristics [13]..

Dark current of the photodiode is further studied by temperature dependent measurements. Current-voltage characteristics with different temperatures from -40 ℃ to 180 ℃ (Figure 3.4. (a)). From the temperature dependent measurement, the activation energy of the dark current is measured at a reverse bias voltage of -1 V. Extracted activation energy of 0.36 eV, which is approximately half of the Ge bandgap, suggesting that the dominating mechanism for the dark current is Shockley-Read-Hall (SRH)

generation (Figure 3. 4. (b)). The result confirms that suppressing TDD and having better Ge crystal quality, and separating the defective Si/Ge interface away from the device region, are the keys to lower the dark current. Diode ideality factor is measured as a function of temperature (Figure 3.4. (c), Table 3.1). At room temperature, ideality factor of 1.31 is measured. As temperature increases, ideality factor approaches 1.

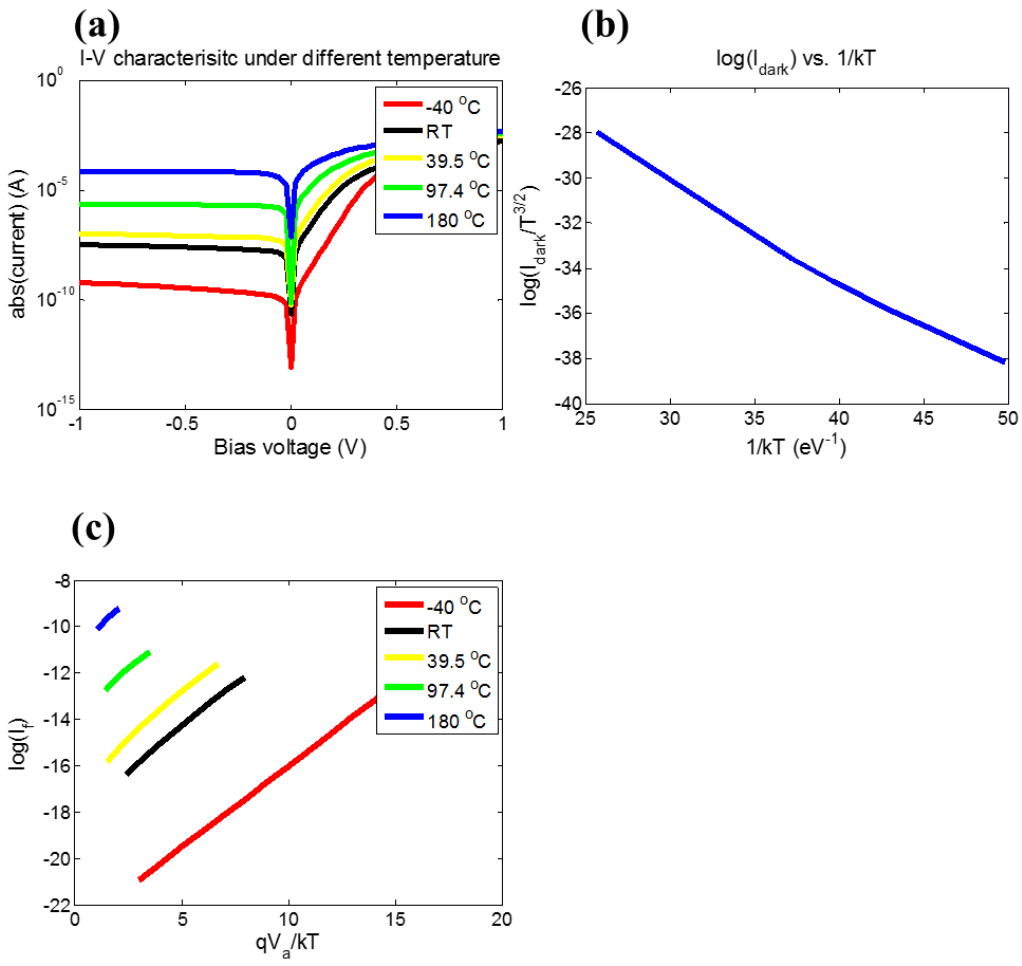

Figure 3.4. Temperature dependent measurement of the photodiode [13].

Temperature (°C)	Ideality factor
-40.0	1.43
20.0	1.31
39.5	1.25
97.4	1.25
180.0	1.16

Table 3.1. Ideality factor of the photodiode as a function of temperature [13].

Optical response of the photodiode is measured by a lock-in based technique. The diode is illuminated from the top. The laser is focused at the center of an i-region of the lateral p-i-n photodiode. Using a supercontinuum light source, wavelength of the laser is varied from 750 nm to 900 nm (Figure 3.5. (a)), and from 1200 nm to 1700 nm (Figure 3.5. (b)). As a comparison, assuming 100 % internal quantum efficiency, responsivity is calculated using a transmission matrix method. For the transmission matrix model calculation, measured thicknesses of 510 nm Ge and 920 nm SiO_2 covered by a passivation stack of 20 nm aluminum oxide (Al_2O_3) and 20 nm low temperature oxide (LTO, SiO_2) are used. For the Ge layer, refractive index and absorption coefficient of unstrained Ge are used. Since the laser spot size is larger than the width of the i-region, the calculated responsivity is scaled by the portion of the optical power falling onto the i-region. Numerical aperture (NA) microscope objective is 0.42. Using the NA, spot size of the laser is calculated as (wavelength/NA). From the calculated spot size, the laser power

and the responsivity are scaled. Due to the absence of an anti-reflection coating (ARC), external quantum efficiency and the responsivity are limited. By using a proper ARC, responsivity of the device would be greatly improved [8]. High internal quantum efficiency, which could be indicated from the ratio between the measured responsivity to the model calculation assuming 100 % internal quantum efficiency, suggests high GOI crystal quality and decent interface quality. Compared to the model calculation using optical constants of un-strained Ge, due to the residual strain in the lateral overgrowth GOI discussed in Chapter 2, red shift of absorption edge is observed (Figure 3.5. (b)). The resulting responsivity spectrum covers the entire C-band. This confirms that lateral overgrowth GOI based photodiodes do not require additional strain engineering to be sued for optical interconnects.

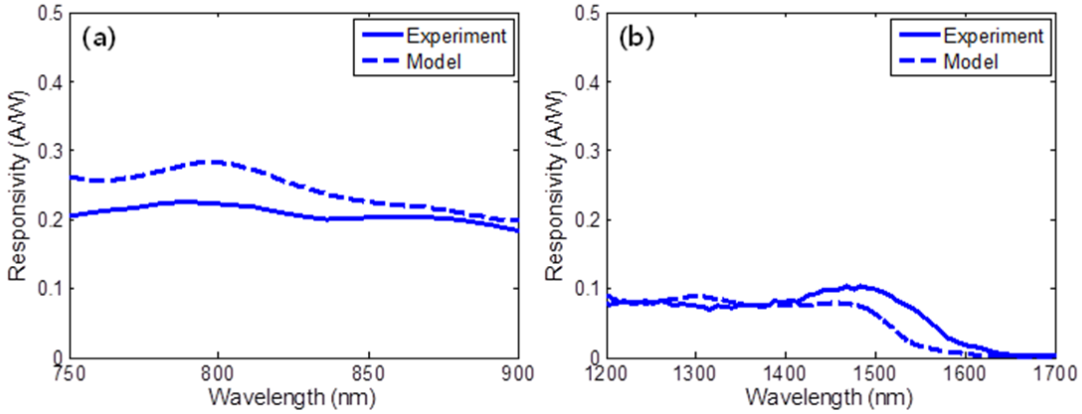

Figure 3.5. Optical response of the photodiode. (a) From 750 nm to 900 nm, and (b) from 1200 nm to 1700 nm. Solid lines are the measured data, and dotted lines are model results from the transmission matrix calculation [13].

3.4 Conclusion

Using the lateral overgrowth technique, GOI based lateral p-i-n photodiode is monolithically integrated on a Si (001) substrate. The resulting photodiode demonstrates excellent characteristics. High on/off ratio, low dark current, and high responsivity suggest high GOI crystal quality and interface quality. Compared to an un-strained Ge based model calculation, responsivity spectrum of the photodiode is extended to cover the entire C-band, due to the residual strain in GOI, without additional strain engineering.

REFERENCE

[1] A. K. Okyay, A. M. Nayfeh, K. C. Saraswat, N. Ozguven, A. Marshall, P. C. McIntyre, and T. Yonehara, "Strain enhanced high efficiency germanium photodetectors in the near infrared for integration with Si," in 9th Annual Meeting of the IEEE Lasers and Electro-Optics Society (LEOS), 2006, 460-461

[2] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Claus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zwadzki, S. Thompson, and M. Bohr, "A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors," in Electron Devices Meetings, 2003, 11.6.1 – 11.6.3

[3] C. Vu, "IBM Research Alliance Produces Industry's First 7nm Node Test Chips," IBM, retrieved from https://www.ibm.com/ (July 9 2015)

[4] S. J, Koester, G. Dehlinger, J. D. Schaud, J. O. Chu, Q. C. Ouyang, and A. Grill, "Germanium-on-insulator photodetectors," in Proceedings of the 2nd IEEE International Conference on Group IV Photonics, 2005, 171-173

[5] M. Oehme, M. Kaschel, J. Werner, O. Kirfel, M. Schmid, B. Bahouchi, E. Kasper, and J. Schulze, "Germanium on silicon photodetectors with broad

spectral range," Journal of the Electrochemical Society 157 (2), H144-H148 (2010)

[6] L. Vivien, J. Osmond, J.-M. Fedeli, D. Marris-Morini, P. Crozat, J.-F. Damlecourt, E. Cssan, Y. Lecunff, and S. Laval, "42 GHz p.i.n Germanium photodetector integrated in a silicon-on-insulator waveguide," Optics Express 17 (8), 6252-6257 (2009)

[7] S. J. Koester, L. Schares, C. L. Schow, J. D. Schaub, G. Dehlinger, and J. O. Chu, "Ge-on-insulator photodetectors for high-speed optical interconnects," in 210th ECS Meetings, 2006, 1402

[8] S. J. Koester, J. D. Schaub, G. Dehlinger, and J. O. Chu, "Germanium-on-SOI infrared detectors for integrated photonic applications," IEEE Journal of Selected Topics in Quantum Electronics 12 (6), 1489-1502 (2006)

[9] G. Wang, R. Loo, E. Simoen, L. Souriau, M. Caymax, M. M. Heyns, and B Blanpain, "A model of TDD in strain-relaxed Ge and GaAs epitaxial films on Si (100)," Applied Physics Letters 94, 102115 (2009)

[10] J. H. Nam, S. Alkis, D. Nam, F. Afshinmanesh, J. Shim, J.-H. Park, M. brongersma, A. K. Okyay, T. I. Kamins, and K. C. Saraswat, "Lateral overgrowth of germanium for monolithic integration of germanium-on-insulator on silicon," Journal of Crystal Growth 416, 21-27 (2015)

[11] J. H. Nam, T. Fuse, Y. Nishi, and K. C. Saraswat, “Germanium on insulator (GOI) structure using hetero-epitaxial lateral overgrowth on silicon,” ECS Transactions 45 (4), 203-208 (2012)

[12] J. H. Nam, W. S. Jung, J. Shim, T. Ito, Y. Nishi, J.-H. Park, and K. C. Saraswat, “Germanium on insulator (GOI) structure locally grown on silicon using hetero epitaxial lateral overgrowth,” in 2013 IEEE SOI-3D Subthreshold Microelectronics Technology Unified Conference (S3S), 2013

[13] J. H. Nam, F. Afshinmanesh, D. Nam, W. S. Jung, T. I. Kamins, M. L. Brongersma, and K. C. Saraswat, “Monolithic integration of germanium-on-insulator p-i-n photodiode on silicon,” Optics Express 13 (12), 15816-15823 (2015)

Chapter 4:

Ge metal-insulator-semiconductor photodiode

For high bandwidth optical interconnects, metal-semiconductor-metal (MSM) photodiodes have been studied and demonstrated. For Ge based optical applications, due to high dark current, MSM photodiodes have not been under active use. In this chapter, a Ge metal-insulator-semiconductor (MIS) photodiode is suggested and demonstrated by utilizing a carrier-selective de-pinning insulting layer. Resulting photodiode demonstrates more than three orders of magnitude lower dark current compared to a conventional MSM photodiode with same dimensions, while preserving the optical response.

4.1 MSM photodiodes

For high bandwidth optical interconnect systems, MSM photodiodes have been under active study. Schematic energy band diagram of the device is shown in Figure 4.1. MSM photodiode consists of two meal-semiconductor (MS) Schottky junctions connected back-to-back. Without illumination, electrons and holes are blocked at the Schottky

junctions, and the resulting dark current is low. When the device is illuminated with bias voltage applied, electron hole pairs are generated in the semiconductor region. Generated electrons and holes are separated by the applied field, and collected by the metal contacts.

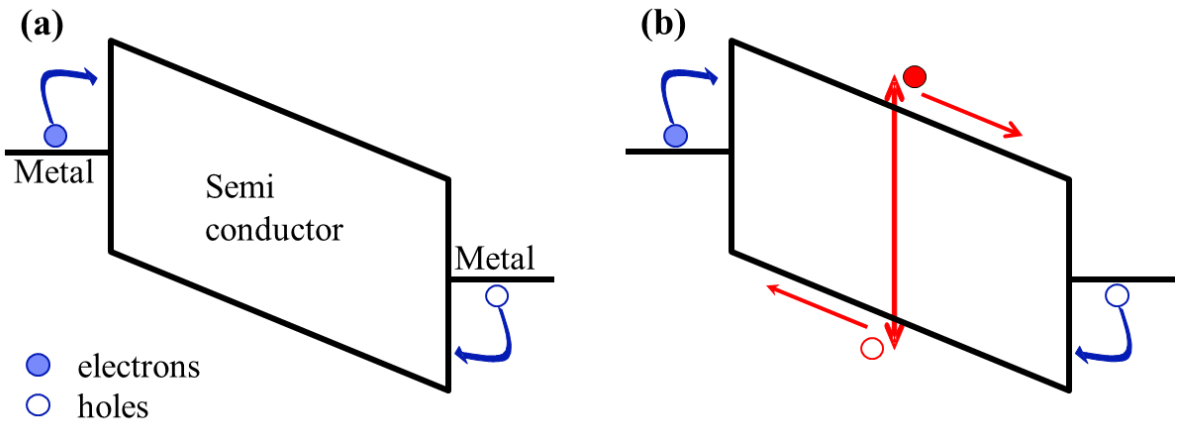

Figure 4.1. Energy band diagram of MSM photodiode under bias. (a) Without illumination. Dark current is blocked by Schottky junctions at the MS junctions. (b) With illumination. Electrons and holes are generated by illumination (marked red), are separated by the applied field, and collected at the metal contacts.

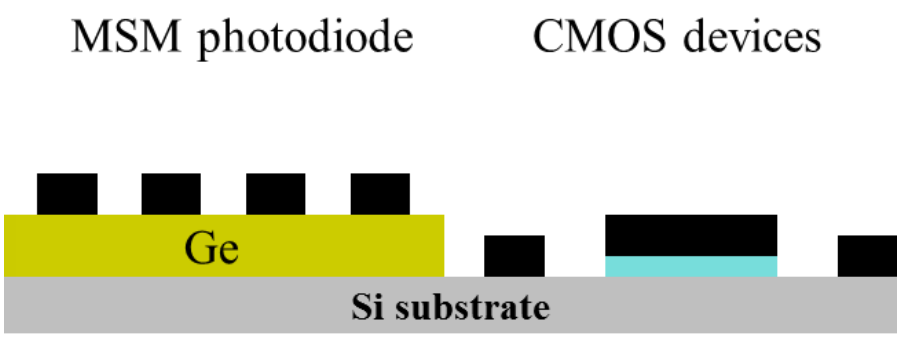

Figure 4.2. Integration of MSM photodiodes with CMOS devices.

MSM photodiodes, compared to another common option, p-i-n photodiode, first of all, has much simpler device structure. MSM photodiode is composed of a semiconductor with proper optical band gap, and two metal contacts. MSM photodiode does not require ion implantations, and subsequently, requires less number of lithography steps. Absence of high temperature thermal annealing to remove implant damage enhances thermal budget of the process. Planar overall structure makes integration of MSM photodiodes with CMOS devices easier.

Device performance-wise, especially compared to vertical p-i-n photodiode, MSM photodiode has intrinsically low parasitic junction capacitance. Due to the low RC delay, MSM photodiode can achieve higher operation speed and bandwidth [1].

To conclude, easy integration with CMOS devices and expected high-speed and bandwidth makes MSM photodiode an ideal structure for high performance optical interconnects. High performance MSM photodiodes based on III-V compound semiconductors have been demonstrated [1-3]. But, for Ge based optics, MSM

photodiodes have not been under active study, largely due to high dark current [4]. When a metal is contacted to a semiconductor, the metal Fermi level tends to get pinned to a specific point within the semiconductor bandgap at the contact. For Si, and for some of the III-V compound semiconductors, this pinning happens deep inside the band gap. When a MSM photodiode is made, enough energy barriers are provided for electrons and holes at the MS junctions, and the dark current is low (Figure 4.3. (a)). For Ge, unfortunately, this pinning happens very close to the valence band of Ge, and when an MSM diode is made, the resulting energy barrier for holes is very small. As a result, Ge MSM photodiode suffers from high dark current due to hole injection (Figure 4.3. (b)).

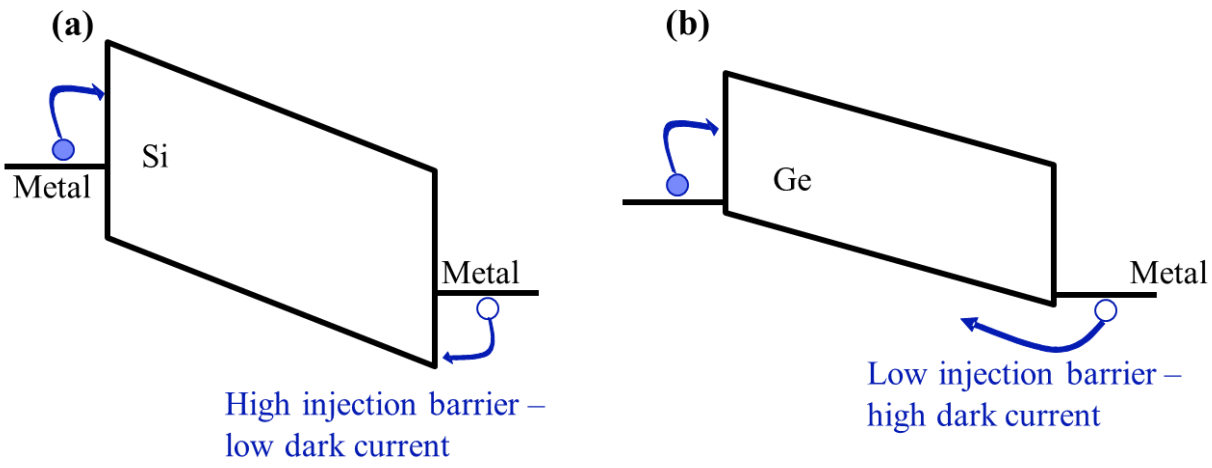

Figure 4.3. MSM photodiodes on (a) Si and (b) Ge. For Si, Fermi level pinning happens close to mid-gap, providing sufficient energy barriers for both electrons and holes. For Ge, Fermi level pinning happens close to valence band of Ge, and high hole injection current occurs.

On a 500 nm lateral overgrowth GOI discussed in Chapter 2 and Chapter 3, MSM photodiode is demonstrated. Compared to a lateral p-i-n photodiode with same dimension (Figure 4.4), MSM photodiode shows about 5 orders of magnitude higher dark current (Figure 4.5). This high dark current makes practical use of Ge based MSM photodiodes problematic.

To suppress the dark current, utilizing different contact metals has been tried [4]. By using lower work function metal, increasing the injection barrier for the holes has been tried. By changing the contact metal from Ni to Ti, work function of the metal has been lowered by ~1 eV. Actual dark current has been suppressed only by ×2, due to the strong Fermi level pinning [4]. From this study, it can be concluded that to suppress the dark current effectively, the metal Fermi level needs to be de-pinned.

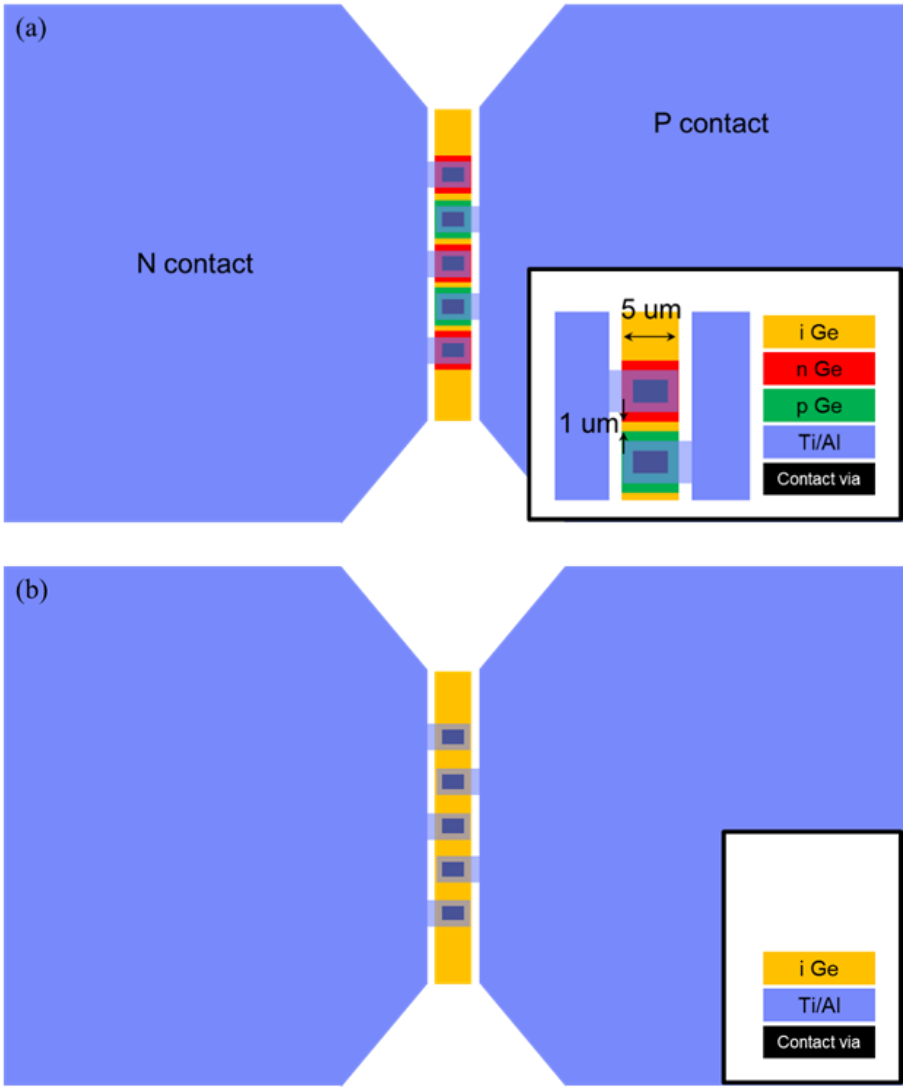

Figure 4.4. (a) Lateral p-i-n photodiode and (b) MSM photodiode fabricated on 500 nm lateral overgrowth GOI.

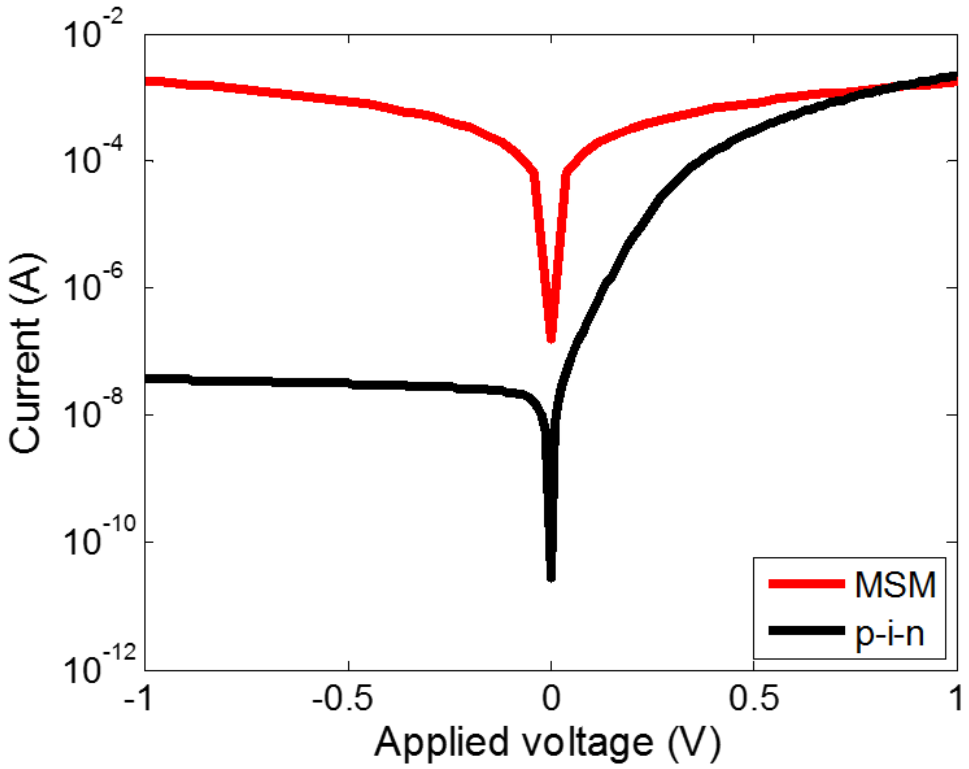

Figure 4.5. Current-voltage characteristics of MSM and p-i-n photodiodes. The MSM photodiode shows ~5 orders of magnitude higher dark current than the p-i-n photodiode of comparable dimension (Figure 4.4).

4.2 Fermi level pinning and de-pinning

To de-pin the Fermi level, what is causing the pinning needs to be understood. Figure 4.6 shows an energy band diagram of an MS junction. By defining the work function of the metal as φ_m and electron affinity of the semiconductor as χ, without any interface states, Schottky barrier height of electrons can be written as:

$$\Phi_{Bn} = \varphi_m - \chi.$$

If there are interface states, the barrier height changes. Constant interface state density of D_{is} throughout the entire band gap of the semiconductor is assumed. By defining a charge neutrality level as E_{CNL} at which the interface states change from donor like to acceptor like and Fermi level at equilibrium as E_F, total interface charge can be written as:

$$-q \cdot (E_F - E_{CNL}).$$

Assuming a thin vacuum layer with thickness δ between the metal and the semiconductor, by following the model, Schottky barrier height can be expressed as:

$$\Phi_{Bn} = S(\varphi_m - \chi) + (1 - S)\Phi_{B0},$$

by defining

$$S = \left(1 + \frac{q^2}{\varepsilon_i \varepsilon_0} D_{IS} \delta\right)^{-1},$$

and

$$\Phi_{B0} = E_{CB} - E_{CNL}$$

where q is the electric charge, ε_0 is the permittivity of free space, and ε_i is the dielectric constant of the inteface layer.

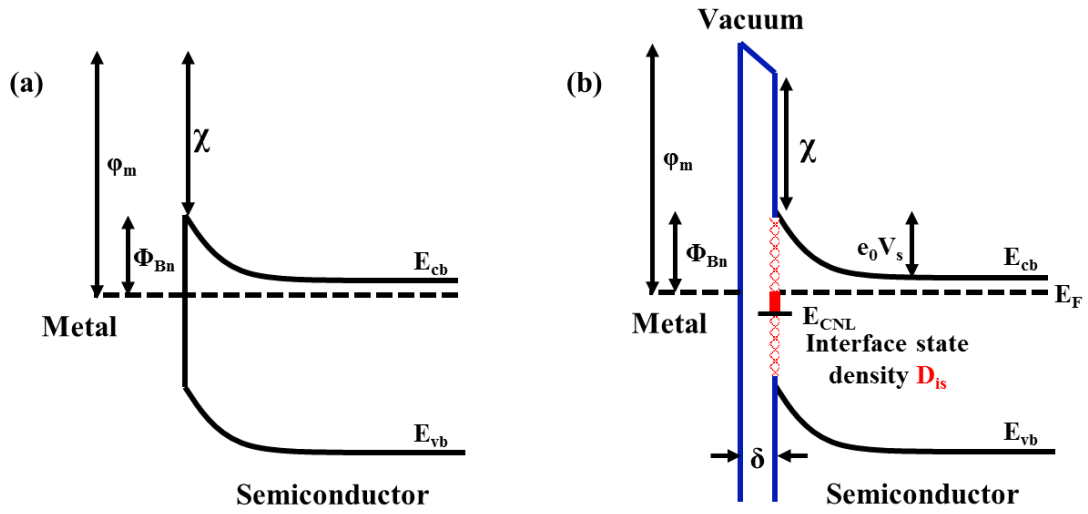

Figure 4.6. Energy band diagram of MS junction (a) MS junction without interface states. (b) MS junction with interface states [5].

From the expression, it can be seen that if the interface state density is low, the parameter S approaches 1, and the barrier height Φ_{Bn} approaches $\varphi_m - \chi$. In this case, the barreir height can be easily changed by changing the metal work function, and the Fermi leve is not pinned. If the interfce state density is very high, the parameter S approaches 0, and Φ_{Bn} approaches $\Phi_{B0} = E_{CB} - E_{CNL}$. When this happens, the barrier height Φ_{Bn} becomes more and more independent of the metal work function φ_m, and the Fermi level is now pinned to the charge neutraliti level, E_{CNL}. And the parameter S is defined as pinning factor [5].

From the discussion above, it can be concluded that interface states cause Fermi level pinning. Now, how the interface states are generated needs to be understood. There is an on-going discussion about the physical understandings on the interface state generation

[5-8]. Among the models explaining the interface states, here, metal induced gap states (MIGS) model is discussed [5-7].

For a bulk-like semiconductor, model of the energy band structure is based on an assumption that the semiconductor crystal is infinite. In the bulk-like semiconductor, Schrödinger's equation is solved for real wave vectors, since solutions with imaginary wave vectors cannot be normalized, and have no physical meaning [5]. On the other hand, when a MS junction is made, solutions with imaginary wave vectors have physical meanings.

Figure 4.7 shows an energy band diagram of a model semiconductor, with a linear chain with lattice parameter a. When a MS contact is made, the imaginary component of the wave vector generates states within the band gap [5]. At the MS junction, when the conduction band of the metal overlaps with the band gap of the semiconductor, electron wave function from the metal side penetrates into the semiconductor. The wave function decays exponentially inside the semiconductor, and strictly confined to the interface. The model is named as metal-induced gap states (MIGS).

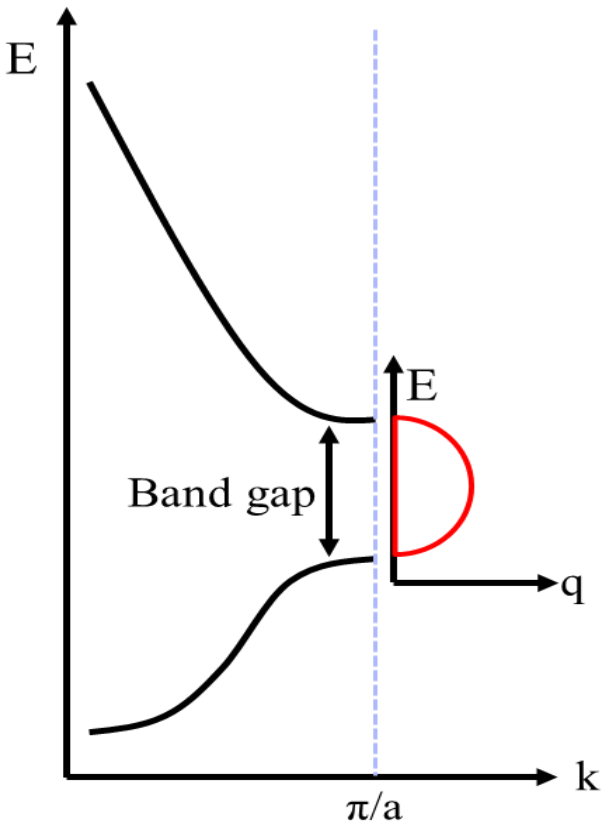

Figure 4.7. Energy band diagram of a model semiconductor, with real (black line) and imaginary (red) wave vectors [5].

From the above discussion, it can be seen that if there are interface states, then there is Fermi level pinning. And, when a semiconductor is contacted to metal, interface states are generated due to the electron wave function penetration from the metal side into the semiconductor side. To de-pin the Fermi level at the junction, insertion of a wide band gap material between the metal and the semiconductor has been suggested [9]. The MIGS density decays fast within the wide bandgap material, leaving very small density of

interface states at the semiconductor surface [9]. Within the interface layer, decay length of the MIGS density can be expressed as:

$$\delta_{IL} = \frac{h^2}{2\pi m_0 a E_g}$$

where h is the Planck's constant, a is the lattice constant, and E_g is the band gap energy [5, 9]. With increasing interface layer thickness, MIGS density decays, following

$$D_{MIGS}(t) = D_{MIGS0IL} e^{-\frac{t}{\delta_{IL}}},$$

where t is the interface layer thickness, and $D_{MIGS0IL}$ is the MIGS density with zero interface layer thickness, which can be expressed as

$$D_{MIGS0IL} = \frac{2}{\pi a^2 E_g}.$$

Due to the decay of the MIGS density, effective pinning factor of the MIS junction can be expressed as

$$S = \left(1 + \frac{\varepsilon_{IL}(1 - S_{IL}) e^{-\frac{t}{\delta_{IL}}} (\delta_S \varepsilon_{IL} + t\varepsilon_S)}{S_{IL}\delta_{IL}(\varepsilon_{IL} + \varepsilon_S)}\right)^{-1},$$

where ε_s is the dielectric constant of the semiconductor [9]. From the above discussion, it can be concluded that the pinning factor S can approach to 1, by using a large bandgap interface de-pinning layer, or by increasing the thickness of the interface de-pinning layer [9]. By using wide bandgap materials such as Al_2O_3, GeO_2, Si_3N_4, and TiO_2, effective de-pinning on a metal to germanium contact has been demonstrated [9].

4.3 MIS photodiode

It has already been demonstrated that by inserting a wide bandgap material between the metal and the semiconductor, it is possible to de-pin the Fermi level [9-10]. Through this de-pinning, and by carefully choosing a small work function contact metal, reduction of the dark current of the Ge MSM photodiode can be achieved (Figure 4.8. (a)-(b)).

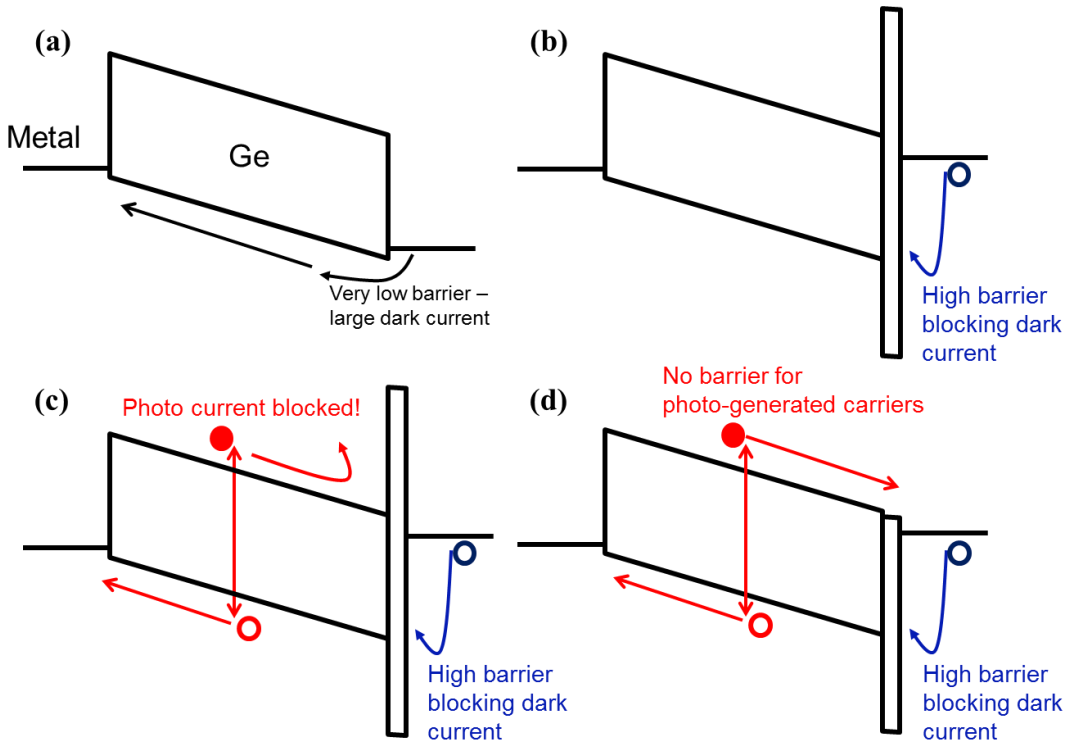

Figure 4.8. MIS photodiode. (a) MSM photodiode with strong Fermi level pinning. (b) Dark current blocking with MIS photodiode. (c) Photo current blocking in MIS photodiode. (d) MIS photodiode with carrier selective de-pinning layer.

Any wide bandgap material can be used for the MIS de-pinning, and the dark current suppression (Figure 4.8. (b)). But, if the inserted de-pinning layer has high conduction

band energy offset to Ge, when light is illuminated on the photodiode, the photo-generated electron current is also blocked (Figure 4.8. (c)), and the responsivity of the photodiode suffers. This can be avoided by choosing a de-pinning layer without or with negative conduction band offset to Ge. Photo-generated electrons do not see any additional barrier, and the responsivity is not affected (Figure 4.8. (d)). By using the carrier selective de-pinning layer which allows electrons from Ge to pass without any barrier, dark current can be suppressed by de-pinning and valence band offset of the de-pinning layer to Ge and the metal, while preserving the photocurrent and the responsivity of the photodiode.

Among various wide bandgap materials, TiO_2 provides negative conduction band offset to Ge (-0.06 eV), while providing wide enough bandgap energy of 3.05 eV for effective de-pinning (Table 4.1).

Material	Bandgap (eV)	Conduction band offset to Ge (eV)
SiO_2	8.9	3.1
Si_3N_4	5.1	1.8
Al_2O_3	8.8	2.8
ZnO	3.4	-0.1
TiO_2	3.05	-0.06

Table 4.1. Various wide bandgap materials. TiO_2 has negative conduction offset to Ge.

4.4 MIS photodiode fabrication

MIS photodiode with a carrier-selective TiO_2 de-pinning layer is integrated on an epitaxially grown Ge on Si (001) substrate. As a comparison, a Ge MSM photodiode with the same dimension, without the TiO_2 MIS contact is fabricated. Schematic figures of the devices are shown in Figure 4.9. Compared to a lateral p-i-n photodiode, MIS photodiode has simpler device structure, with a single TiO_2 de-pinning layer added to one side of the contacts of a simple MSM photodiode. Also, unlike the p-i-n photodiode, the MIS photodiode does not require ion implantations, high temperature annealing, and multiple lithography steps, reducing the integration cost of the device and improving the thermal budget.

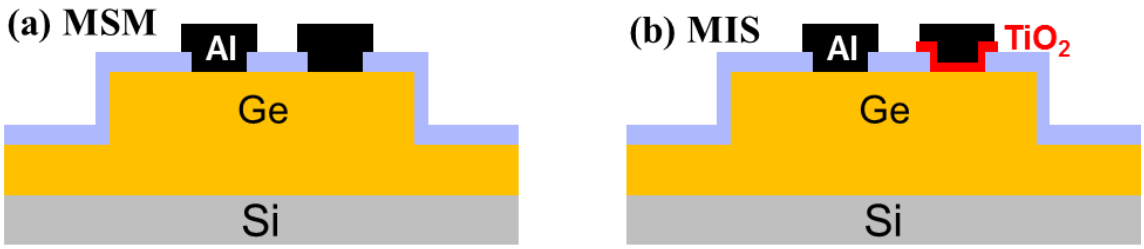

Figure 4.9. MSM and MIS photodiode. MIS photodiode has a thin TiO_2 de-pinning layer on one side of the contact.

For the fabrication, a Si (001) wafer is prepared by HF last RCA cleaning. Immediately after the native oxide removal in HF, the wafer is loaded into an Applied Materials epi Centura reactor. Any remaining native oxide is removed by a high temperature a H_2 bake at 1000 ℃. For a smoother starting surface, thin Si layer is grown epitaxially at 600 ℃

using DCS gas. On the smooth surface, 2 μm Ge is grown hetero-epitaxially. Initial seed layer is grown at 400 ℃ with GeH_4, then annealed with H_2 at 825 ℃. Second layer is grown at 600 ℃, followed by another H_2 annealing at 825 ℃.

Lateral MIS photodiode is fabricated on epitaxially grown Ge. First, using optical lithography and dry etching, 5 μm × 44 μm mesa is defined (Figure 4.10. (a)). After the photoresist removal, the sample is cleaned by cyclic HF cleaning. The Ge surface is passivated by 50 nm ALD Al_2O_3 (Figure 4.10. (b)). Using optical lithography and wet etching using 20:1 HF, de-pinning contact vias are defined. After removing the photoresist, an ALD TiO_2 layer with various thicknesses is deposited by CambridgeNanoTech Savanna system at 200 ℃, using tetrakis (dimethlamido) titanium (IV) and H_2O as precursors (Figure 4.10. (c)). After covering the TiO_2 layer deposited on the de-pinning contact vias by photoresist by optical lithography, TiO_2 is dry etched by SF_6 based chemistry, using the underlying Al_2O_3 as an etch mask (Figure 4.10. (d)). Direct metal-Ge contact vias are defined by an optical lithography and a 20:1 HF wet etching (Figure 4.10. (e)). Contact metal is deposited and defined by lift-off (Figure 4.10. (f)). The MSM control device follows the same fabrication process, except for the TiO_2 deposition and patterning processes (Figure 4.10. (c)-(d)).

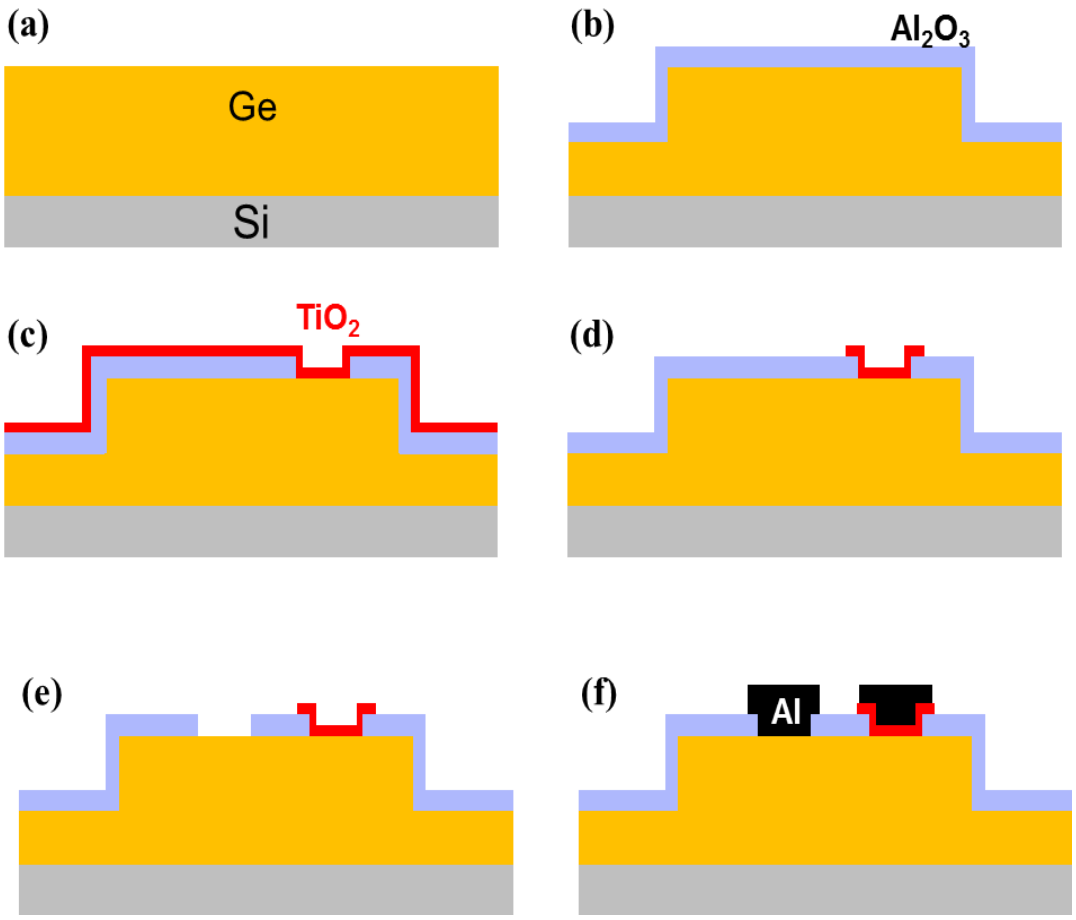

Figure 4.10. MIS photodiode fabrication process flow. (a) Hetero-epitaxially growth of Ge on Si. (b) Mesa definition and Al_2O_3 passivation. (c) MIS contact via definition and an ALD TiO_2 de-pinning layer deposition. (d) TiO_2 patterning. (e) MS contact via definition. (f) Contact metal definition and lift-off.

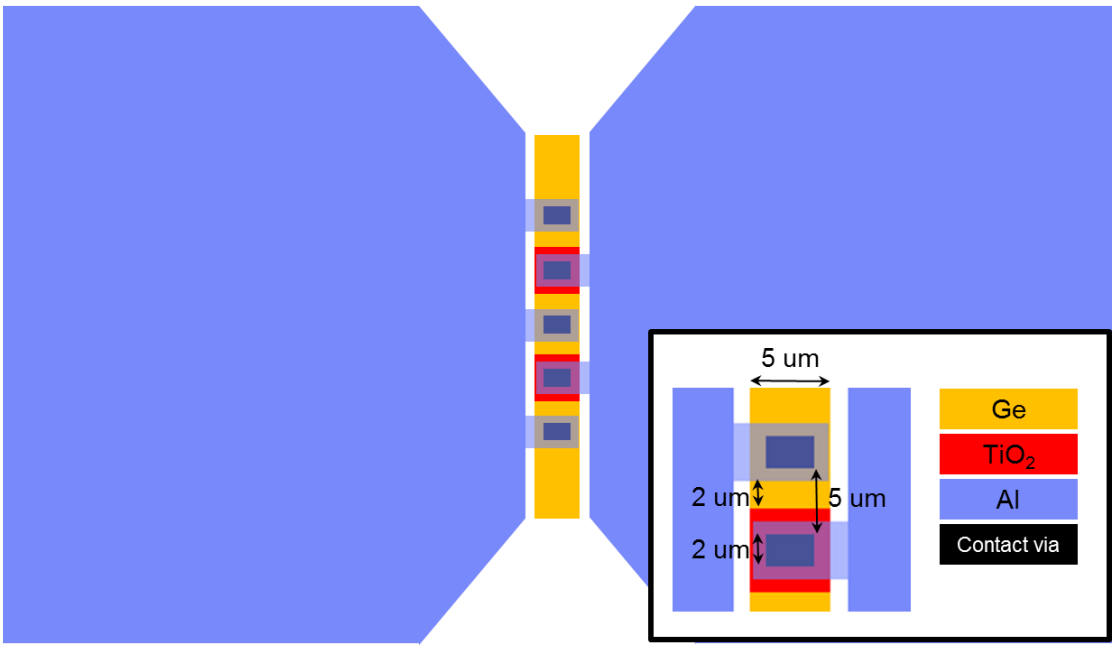

Figure 4.11. MIS photodiode. MSM control device has the same design, except for the TiO_2 de-pinning layer.

Figure 4.11 shows the design parameters of the MIS photodiode and a SEM image of the resulting photodiode.

4.5 Current-voltage characteristics

Current-voltage characteristics of the resulting photodiodes are presented in Figure 4.12. Compared to the MSM control device, MIS photodiode with 10 nm TiO_2 de-pinning layer demonstrates 3×10^3 times lower dark current under the reverse bias operation. The MIS photodiode with 4 nm TiO_2 does not show much improvement over the MSM photodiode. Thickness variation of the ALD TiO_2 is believed to be the reason.

Due the rough surface and the thickness variation, some MIS contact points with thin TiO_2 thickness do not provide enough de-pinning, and forms low resistance paths for dark hole current. Holes flow through those points freely, and causes high dark current comparable to the MSM photodiode.

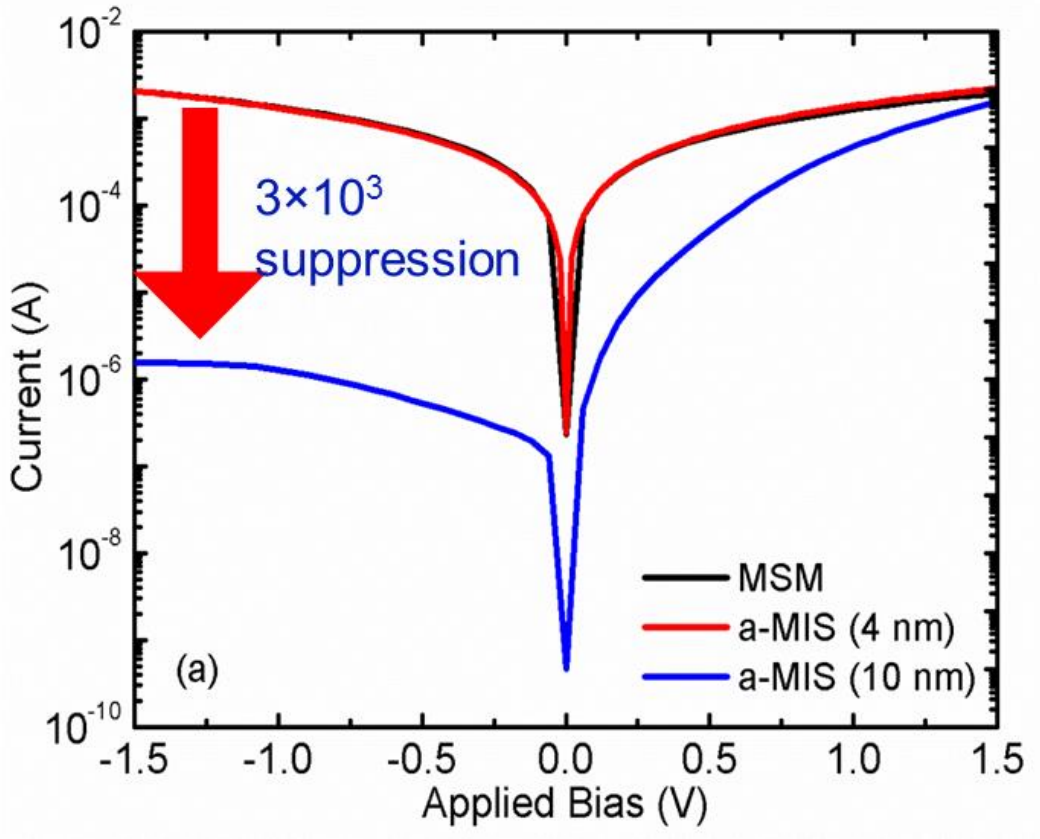

Figure 4.12. Current-voltage characteristics of the MSM and MIS photodiodes with different TiO_2 thicknesses.

For the MIS photodiode with 10 nm TiO_2, de-pinning layer, temperature dependent measurement is conducted.

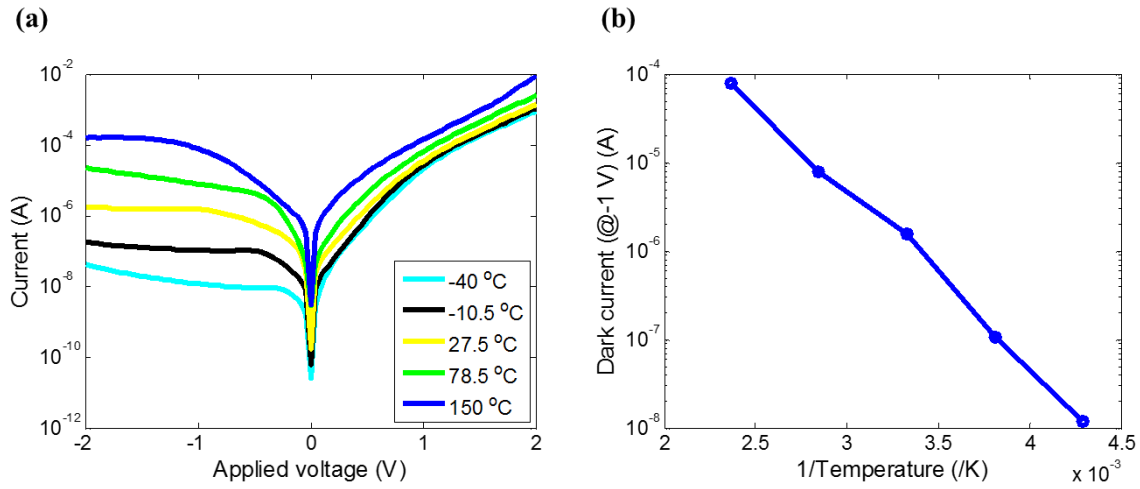

Figure 4.13. Temperature dependent measurement on the MIS photodiode. Measuring temperature is varied from -40 ℃ to 150 ℃.

Figure 4.13 shows the results from the temperature dependent measurement. The measuring temperature is swapped from -40 ℃ to 150 ℃ (Figure 4.13. (a)), and the activation energy of the dark current at -1 V bias is extracted (Figure 4.13. (b)). Measured activation energy of 0.39 eV suggests that the dark current is mainly due to the SRH generation, which confirms hole carrier injection portion of the dark current from the metal contact into Ge is very effectively suppressed by the inserted TiO_2 de-pinning layer (Figure 4.8. (d)).

4.6 Optical responsivity

By using a lock-in base technique, optical responsivity of the MIS and the MSM photodiodes is measured. Laser is illuminated from the top, focusing the region between

the metal contact fingers on the Ge mesa. By using a supercontinuum light source, the laser wavelength is varied from 1200 nm to 1700 nm.

As shown in Figure 4.14, the MIS photodiode demonstrates equal responsivity, compared to the MSM control device. This confirms the inserted TiO_2 does not degrade the photocurrent. From the responsivity measurement (Figure 4.14) and the current-voltage characteristics (Figure 4.12.), it can be concluded that by inserting a carrier-selective TiO_2 de-pinning layer, dark current of the device is successfully suppressed by a factor of 3×10^3, while preserving the photocurrent and the optical responsivity.

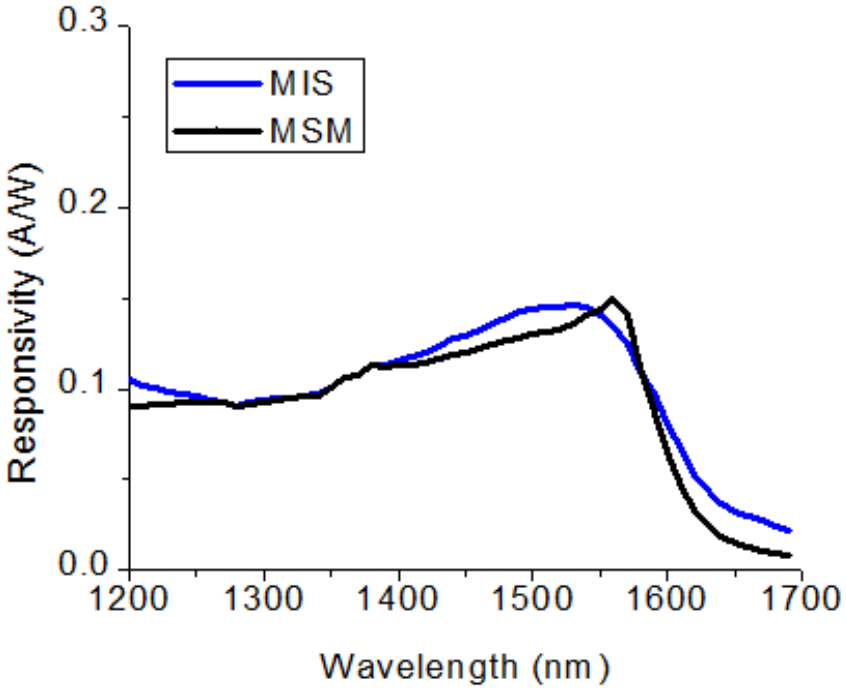

Figure 4.14. Optical responsivity of MIS and MSM photodiodes.

4.7 Effect of TiO_2 stoichiometry

Another interesting observation is made from the diode current-voltage characteristics (Figure 4.12). Following the energy band diagram in Figure 4.8. (d), under a positive bias voltage, due to the valence band offset of TiO_2 to Ge at the MIS junction, both electron and hole currents are blocked, and the expected current is low (Figure 4.15. (b)). On the contrary, the current-voltage characteristics in Figure 4.12 show high current flow under positive bias. This highly suggests hole currents can flow through the TiO_2 layer, despite the high valence band offset of TiO_2 to Ge (Figure 4.15. (c)).

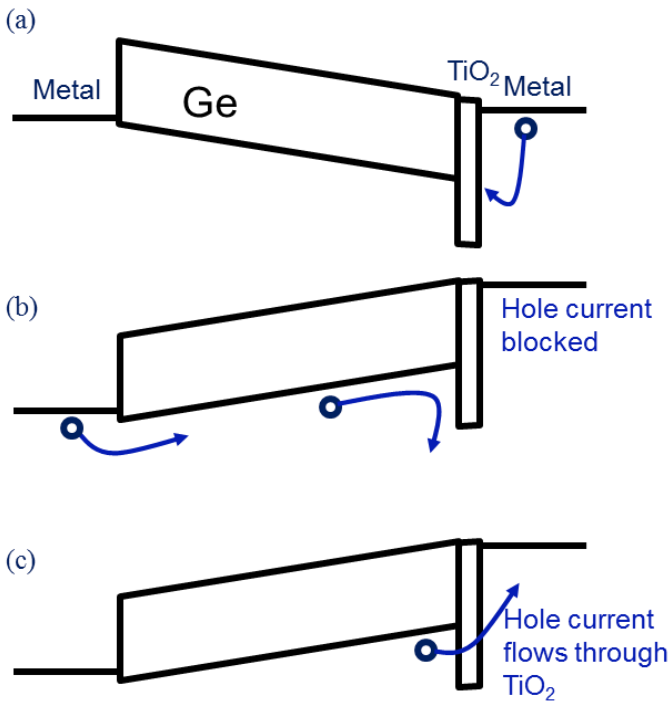

Figure 4.15. Hole dark current in MIS photodiode. (a) Under the reverse bias. (b)-(c) Under the positive bias.

The hole current through TiO_2 can be understood by assuming that oxygen vacancies in the layer provide an alternative current path. When high density of oxygen vacancies are present inside a TiO_2 layer, prior work suggests that the oxygen vacancies generate mid-gap states within the TiO_2 energy bandgap, and hole current can flow through the TiO_2 layer (Figure 4.15. (c)) [11]. X-ray photoelectron spectroscopy (XPS) analysis on the TiO_2 layer confirms high density of oxygen vacancies. Stoichiometry of $TiO_{1.885}$ is measured from the XPS analysis (Figure 4.16. (a)).

Different deposition conditions were studied (Table 4.2) to improve the stoichiometry of TiO_2. By lowering the deposition temperature from 200 ℃ to 150 ℃, stoichiometry is improved from $TiO_{1.885}$ to $TiO_{1.964}$. Plasma ALD at 150 ℃ shows higher stoichiometry of $TiO_{1.998}$.

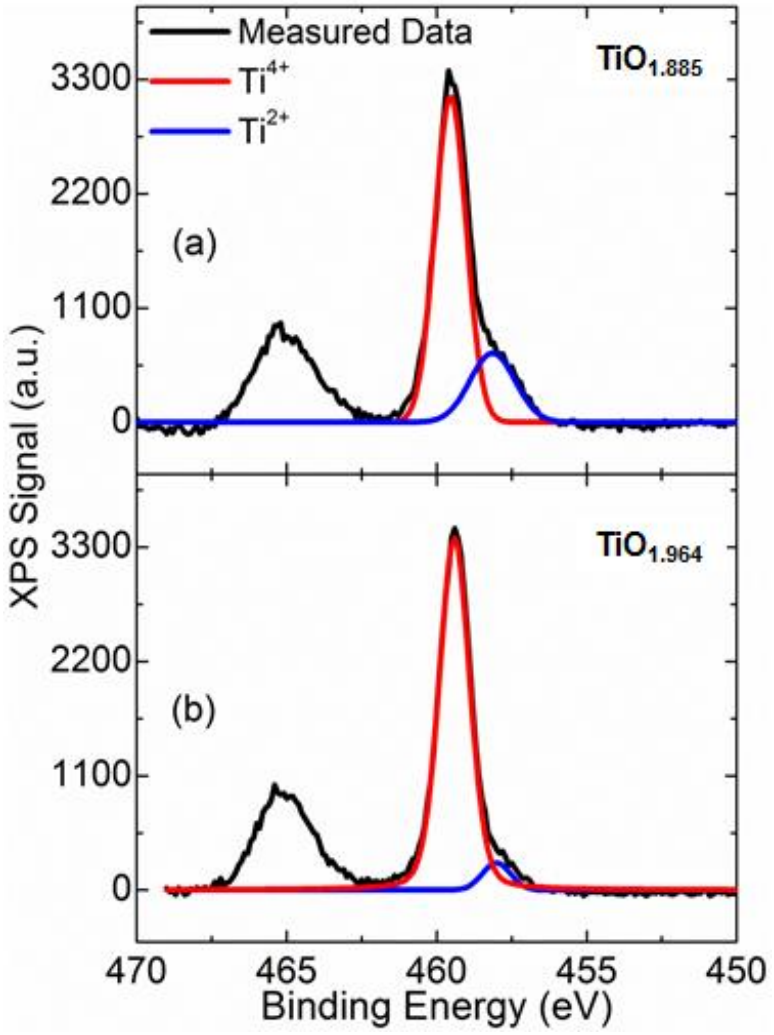

Figure 4.16. XPS analysis on the ALD TiO_x layers. (a) Deposition at 200 ℃. (b) Deposition at 150 ℃.

Other than controlling the deposition condition, stoichiometry of TiO_2 can also be changed by a post-deposition annealing and by plasma deposition. ALD TiO_2 is deposited at 200 ℃, with as deposited stoichiometry of $TiO_{1.885}$. After the deposition, different annealing conditions are tried with varying annealing ambient and temperature.

Results are summarized in Table 4.3. Annealing in N_2 ambient degrades the TiO_2 stoichiometry, since oxygen inside the TiO_2 layer evaporates. Annealing in oxygen ambient improves TiO_2 stoichiometry.

Temp.	**200 ℃**	**150 ℃**	**150 ℃**
ALD Type	**thermal**	**thermal**	**plasma**
X in TiO_x	1.885	1.964	1.998

Table 4.2. Stoichiometry of TiO_x with different deposition conditions.

	As deposited	**200 ℃ O_2 anneal**	**300 ℃ O_2 anneal**	**400 ℃ O_2 anneal**	**300 ℃ N_2 anneal**
X in TiO_x	1.885	1.869	1.948	1.988	1.831

Table 4.3. Stoichiometry of TiO_X with different post annealing conditions.

Current-voltage characteristics of the 10 nm TiO_X MIS photodiodes with different stoichiometry are measured (Figure 4.17). By changing the deposition temperature from 200 ℃ to 150 ℃, stoichiometry of TiO_X is improved from $TiO_{1.885}$ to $TiO_{1.964}$ (Figure 4.16 and Table 4.2). With the improved stoichiometry with fewer oxygen vacancies in the TiO_X layer, a clear decrease in the forward bias dark current is observed. Reverse bias dark current does not change much with the stoichiometry. From the measurement, it can

be concluded that by improving the stoichiometry of TiO_X and reducing the oxygen vacancies, TiO_2 becomes more carrier-selective and hole-blocking.

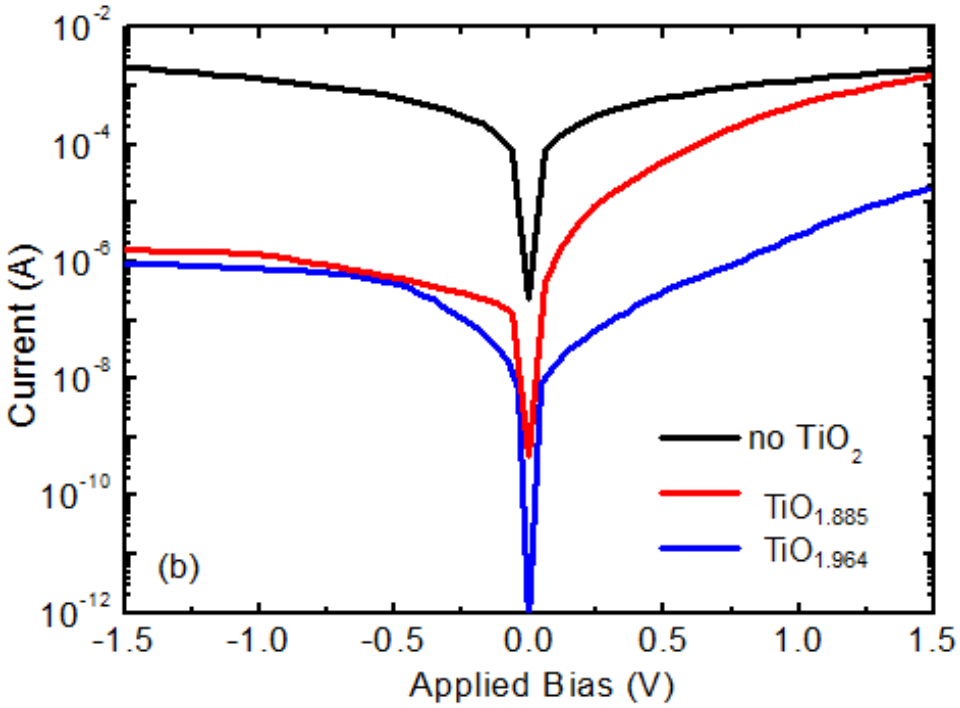

Figure 4.17. Current-voltage characteristics of the MIS photodiodes with different TiO_2 stoichiometry. Current-voltage characteristics of the MSM photodiode is also plotted.

4.8 Further discussion on the dark current

Figure 4.18 is the comparison of current-voltage characteristics of the lateral p-i-n photodiode discussed in Chapter 3, the MIS photodiode, and the MSM photodiode.

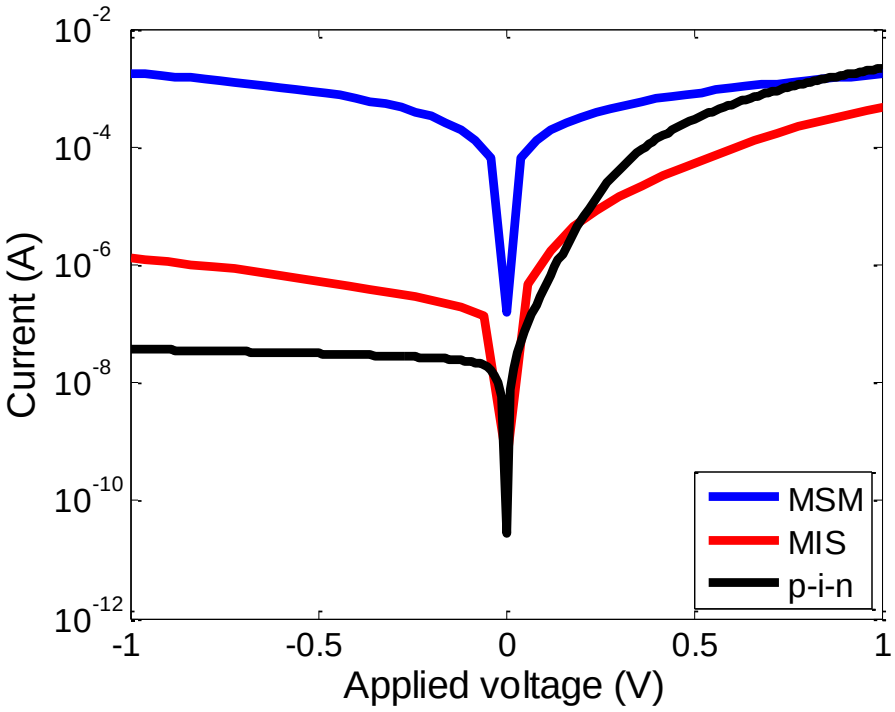

Figure 4.18. Current-voltage characteristics of the lateral p-i-n photodiode (discussed in Chapter 3), the MIS photodiode, and the MSM photodiode.

To further investigate the cause of the dark current, two identical MIS photodiodes are fabricated, one on a 2 μm epitaxial Ge on Si, and the other on a Ge wafer. Current – voltage characteristics of the two devices are compared (Figure 4.19). If the dark current is mainly generated by SRH generation within Ge, since epi-Ge suffer from threading dislocations from Si/Ge interface, it is likely that the epi-Ge would have more SRH generation, and have higher dark current. The two photodiodes show comparable dark currents. The measurement suggests that the main mechanism of the device is not the carrier generation from the Ge bulk. The MIS photodiode shows higher dark current

compared to the lateral p-i-n photodiode with comparable dimension with same Ge surface passivation (ALD Al_2O_3). This again suggests the dominating source of the dark current is not the Ge surface passivation. From the measurements, it could be suggested that the dark current could be mainly coming from the MIS interface.

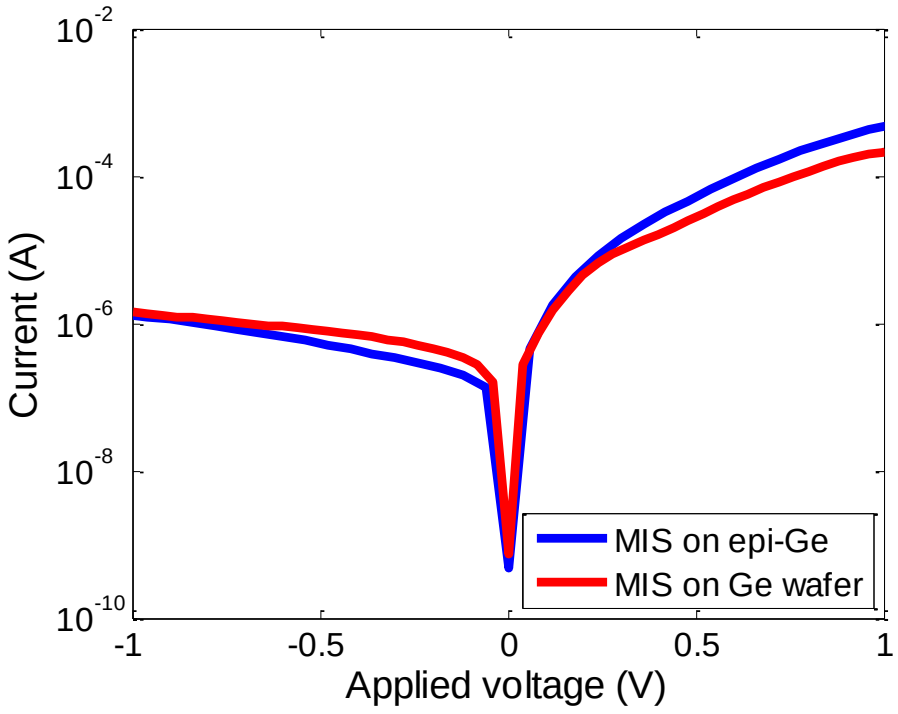

Figure 4.19. Current-voltage characteristics of MIS photodiodes on an epitaxial Ge and on Ge wafer.

The issue of passivating TiO_2 to Si interface has been intensively studied [12-14], with much improvement on the TiO_2/Si interface. For the Ge MIS photodiode, the same

techniques to improve the interface could be tried to further improve the dark current characteristics.

4.9 Conclusion

MIS photodiodes with low dark current are suggested and demonstrated. Compared to a lateral p-i-n photodiode, MIS photodiode has simpler device structure with lower integration cost and improved thermal budget. Compared to an MSM photodiode, by inserting a thin TiO_2 de-pinning layer, dark current of a Ge MSM photodiode is suppressed by a factor of 3×10^3, while preserving a same level of photocurrent and optical responsivity. With improved stoichiometry, the TiO_2 layer becomes more carrier-selective and hole blocking.

REFERENCE

[1] J. B. D. Soole and H. Schumacher, "InGaAs metal-semiconductor-metal photodetectors for long wavelength optical communications," IEEE J. of Quantum Electronics 27 (3), 737-752 (1991)

[2] J. B. D. Soole, H. Schumacher, R. Esagui, and R. Bhat, "Waveguide integrated MSM photodetector for the 1.3μm-1.6μm wavelength range," in IEEE International Electron Devices Meeting (IEDM), 1988, 483-486

[3] S.-W. Seo, S.-Y. Cho, S. Huang, A. Brown, N. M. Jokerst, "High-speed InGaAs thin film MSM photodetector characterization using a fiber-based electro-optic sampling system," Proc. SPIE 5353, Semiconductor Photodetectors 48 (2004)

[4] A. K. Okyay, A. M. Nayfeh, K. C. Saraswat, T. Yonehara, A. Marshall, and P. C. McIntyre, "High-efficiency metal-semiconductor-metal photodetectors on heteroepitxially grown Ge on Si," Optics Letters 31 (17), 2565-2567 (2006)

[5] W. Mönch, "On the physics of metal-semiconductor interfaces," Rep. Prog. Phys. 53, 221-278 (1990)

[6] V. Heine, "Theory of surface states," Physical Review 138, A1689 (1965)

[7] J. Tersoff, "Schottky brrier heights and the continuum of gap states," Physical Review Letters 52, 465 (1984)

[8] R. T. Tung, "Formation of an electric dipole at metal-semiconductor interfaces," Physical Review B 64, 205310 (2001)

[9] S. Gupta, P. P. Manik, R. K. Mishra, A. Nainani, M. C. Abraham, and S. Lodha, "Contact resistivity reduction through interfacial layer-semiconductor contacts," Journal of Applied Physics 113, 234505 (2013)

[10] D. Connelly, C. Faulkner, D. E. Grupp, and J. S. Harris, "A New Route to Zero-Barrier Metal Source/Drain MOSFETs," IEEE Transactions on Nanotechnology 3 (1), 98-104 (2004)

[11] H. Seo, L. R. Baker, A. Hervier, J. Kim, J. L. Whitten, and G. A. Somorjai, "Generation of highly n-type titanium oxide using plasma fluorine insertion," Nano Letters 11, 751-756 (2011)

[12] B. S. Richards, J. E. Cotter, and C. B. Honsberg, "Enhancing the surface passivation of TiO_2 coated silicon wafers," Applied Physics Letters 80, 1123 (2002)

[13] D. Suh, D.-Y. Choi, and K. J. Webber, "Al_2O_3/TiO_2 stack layers of effective surface passivation of crystalline silicon," Journal of Applied Physics 114, 154107 (2013)

[14] J. Jhaveri, S. Avasthi, G. Man, W. E. McClain, K. Nagamatsu, A. Kahn, J. Schwarts, and J. C. Sturm, "Hole-blocking crystalline-silicon/titanium-oxide heterojunction with very low interface recombination velocity," 2013 IEEE 39th Photovoltaic Specialists Conference (PVSC) 3292-3296 (2013)

Chapter 5:

Conclusion

5.1 Summary of contributions

Germanium is a very promising material for high performance CMOS and optical devices.

In chapter 2, a lateral overgrowth technique using SiO_2 as growth mask for monolithic integration of high crystal quality GOI on Si substrate is demonstrated, and the resulting GOI platform characterized. A growth model and kinetics of Ge during a hetero-epitaxial growth, selective growth, and lateral overgrowth are studied with experimental results. The lateral overgrowth typically suffers from polycrystalline Ge nucleation on the SiO_2 growth mask, and void formation at the Ge coalescence point. By using HCl as an etchant gas during the growth, growth selectivity of Ge on SiO_2 is drastically improved, and nucleation is suppressed. By carefully engineering the growth conditions during the lateral overgrowth, void formed at the coalescence point is eliminated. By ART and defect necking, threading dislocations are confined away from the GOI device region.

The lateral overgrowth also separates the defective Si/Ge interface from the GOI device region. From this study, high crystal quality lateral overgrowth GOI free of polycrystalline nucleation and voids is achieved. The lateral overgrowth gives high quality GOI with lower threading dislocation density compared to Ge directly grown on Si or SOI. Due to the high crystal quality and by separating the defective Si/Ge interface away from the GOI region, the lateral overgrowth GOI gives high minority carrier lifetime and higher photoluminescence compared to Ge directly grown on Si or SOI. Lateral overgrowth GOI also has residual tensile strain coming from the thermal expansion mismatch between Ge and Si. As a result, the energy band gap of Ge shrinks, and the lateral overgrowth GOI can be used for C-band optical interconnect systems without further strain engineering. Lateral overgrowth technique is further extended for monolithic integration of GON on Si. Starting from the lateral overgrowth GOI, SiO_2 growth mask is selectively wet etched using BOE.

In chapter 3, a lateral p-i-n photodiode is demonstrated on the lateral overgrowth GOI. Lateral p-i-n photodiodes integrated on Ge grown on Si or SOI for optical interconnects have suffered from high dark current due to the defective quality of GOI and the defective Si/Ge interface beneath the GOI devices. By improving the crystal quality of the GOI and separating the defective Si/Ge interface away from the device, the lateral p-i-n photodiode integrated on the lateral overgrowth GOI provides low dark current and high responsivity.

In chapter 4, an MIS photodiode is demonstrated. Conventional MSM photodiode shows high bandwidth with low integration cost, but Ge based MSM photodiodes suffer

from high dark current. Strong Fermi level pinning at metal to Ge contact pins the metal Fermi level very close to the Ge valence band, providing very low injection barrier to holes from the metal contact into Ge. By forming a MIS contact at one side of the contact of Ge MSM photodiode, by inserting a TiO_2 carrier-selective de-pinning layer between the metal contact and the Ge, dark current of the photodiode is suppressed by a factor of 3×10^3, while preserving the optical responsivity of the photodiode. Compared to a lateral p-i-n photodiode, the MIS photodiode has simpler device structure and lower thermal budget, and is expected to benefit from lower integration cost. Extracted activation energy of the photodiode dark current highly suggests the dominant mechanism of the dark current generation in the new MIS photodiode is SRH generation, which confirms that the inserted de-pinning layer effectively blocks the hole injection from the metal contact into Ge. Carrier selectivity of the photodiodes is studied. It has been demonstrated that by improving the stoichiometry of TiO_2 and reducing the oxygen vacancies, TiO_2 becomes more electron selective and hole blocking, resulting in a significant reduction of dark current.

5.2 Suggestions for future work

Lateral overgrowth provides an ideal platform to monolithically integrate GOI based CMOS devices on Si, including Ge FinFETs and Ge gate-all-around FETs. Using the technique, high performance GOI CMOS devices can be integrated side by side with Si or III-V based devices. GON from the lateral overgrowth process opens a window to integrate highly strained Ge based optical devices on Si. So far, such devices were mainly

demonstrated on layer-transferred Ge membranes. With lateral overgrowth, highly strained Ge optical devices could be monolithically integrated with Si based CMOS circuitry.

Studies on the carrier selective MIS junction can be extended to photovoltaic applications. On the other hand, various interface passivation schemes studied for the photovoltaic devices can be used to passivate the MIS interface to achieve even lower dark currents.